A low-power and area-efficient ultrasound receiver using beamforming SAR ADC with CDAC combined delay cell structure for 3-D imaging systems

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Abstract

We present a low-power area-efficient subarray beamforming receiver (RX) structure for a miniaturized 3-D ultrasound imaging system. Given that the delay-and-sum (DAS) and digitization functions consume most of the area and power in the receiver, the beamforming successive approximation register (SAR) analog-to-digital converter (ADC) shares its capacitive digital-to-analog converter (CDAC) with the delay cells. As a result, the delay cells implemented with capacitors are embedded in the CDAC with significant area reduction, further eliminating the need for power-hungry ADC buffers. Furthermore, the dual reference 10-bit SAR ADC reduces the area of CDAC by 32 times, achieving a switching energy reduction of 98.3%, compared to the conventional SAR ADC. As a result, the proposed beamforming SAR ADC, simulated using a 0.18 μm CMOS process, consumes 230 μW per channel, significantly reducing the per channel capacitance.

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Introduction: Endoscopic and catheter-based three-dimensional (3D) ultrasound imaging systems are getting more attention in intravascular ultrasonography and intracardiac echocardiography applications by enabling fast intraoperative ultrasound examinations with relatively low cost and high spatial resolution. The 2D transducers arrays integrated on the pitch-matched ASIC have been implemented as a feasible solution for the implantable miniaturized ultrasound system [1-4]. The critical challenge is to acquire the data from a large number of transducer channels under the stringent requirements of a small array pitch for high spatial resolution and low power consumption to avoid tissue temperature rise. The per-channel ADC makes it challenging to achieve miniaturization, improved spatial resolution, and power efficiency [1]. Subarray analog beamforming effectively reduces the number of ADCs, aligning the echo signals from adjacent transducers by delaying and summing, followed by per-subarray ADCs to lower the channel count for the further digital beamforming operation [2-4].

Given that the DAS and digitization are mainly implemented by a switched capacitor circuit, integrating/summing amplifier, ADC buffer, and SAR ADC [2], the per channel area and power consumption is highly affected by the total capacitance and use of the active circuitry in the sub-array beamformer. The current mode summation with boxcar integration in [3] minimizes the number of capacitive delay cells but still requires the current integrating amplifiers. The DAS is implemented with the charge domain combined with a charge-sharing SAR ADC [4], removing the ADC buffer. However, the SAR ADC suffers from area inefficiency due to its conventional CDAC architecture.

This letter proposes the CDAC combined delay cell (CCDC) structure by sharing the CDAC with the capacitive delay cells for the charge domain summation, eliminating the need for active buffers and amplifiers. Furthermore, the total capacitance of the CDAC is minimized by the dual reference SAR ADC. Consequently, the proposed beamforming SAR ADC is simulated using a 0.18μm CMOS process, consuming 230μW per channel, significantly reducing the total capacitance for high area efficient beamforming.

Overall Architecture: Fig. 1 shows the conventional (Fig. 1a) and proposed (Fig. 1b) sub-array beamforming RX architectures which consist of analog front-ends (AFEs) and beamformers for DAS operation, assuming the number of sub-array is M and 10-bit SAR ADC is utilized for the digitization. The conventional RX requires the switched capacitor delay cells with a capacitance of 2*Cs*N*M, an ADC buffer, and a SAR ADC using CDAC with a capacitance of 2024*C where 1*C is a unit capacitance in CDAC and N is the number of delay cells determining the analog delay range, and Cs is a capacitance of the delay cell. In contrast, the proposed RX exploits the CDAC as delay cells with a CCDC structure, eliminating the power-consuming ADC buffer. In addition, the capacitance of the CDAC is further minimized to 64*C by using a dual-reference (Vref and Vref/32) switching scheme, requiring capacitance of

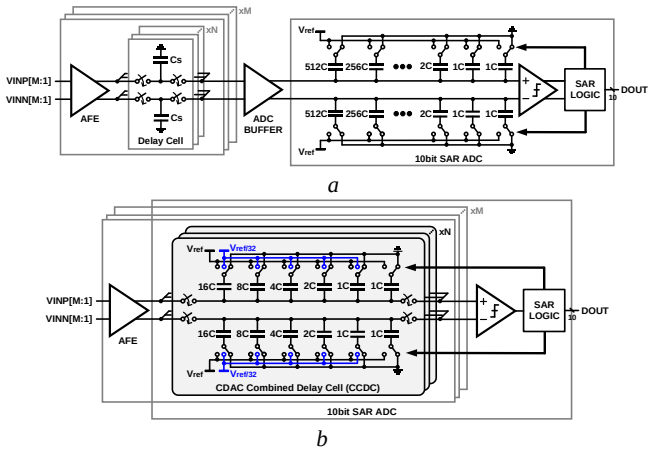

Fig. 1 *Sub-array beamforming RX architecture*
a Conventional architecture
b Proposed architecture with CCDC structure

64*C*N*M for beamforming, while the conventional structure demands capacitance of 2*Cs*N*M+2024*C. Considering the 100fF of Cs in [2] and 24fF of C in [4], and 2fF of C in this work, the proposed beamforming architecture without ADC buffer has an advantage of both power and area efficiencies.

Beamformer Implementation: Fig.2 shows the sub-array beamforming SAR ADC with its timing diagram, assuming the array is divided into sub-arrays of 3 channels where the signals from the focal point are received in channels 1, 2, and 3 with 0, 1, and 3 unit delays, respectively. First, the signals from each channel are sampled and held at CCDC with N sampling capacitors according to the N-phased sampling clocks of S<N-1:0>, where the period of one phase shift is equivalent to the one unit delay. Then, according to the delay profiles of the focal point (0, 1, and 3 unit delays for channels 1, 2, and 3 in the example), the corresponding readout switches are turned on through the readout clocks of R1<0>, R2<1>, and R3<3> at the same time. On the rising edge of readout clocks, the charges of correspondingly delayed cells are averaged (summed) by charge redistribution. After the delayed and summed signal is settled, the comparator starts SAR conversion enabled by asynchronously generated ADC sampling clock CCLK during the readout clock is high.

The total capacitance of the CDAC needs to be minimized so that the proposed CCDC structure has an advantage in the area efficiency over the previous beamformers. Fig. 3 shows low-area CDAC architecture using a dual reference switching scheme. The first and second reference voltage, Vref1 and Vref2, are set to Vref and Vref/2^n, where n is half the m in the m-bit SAR ADC. The MSB capacitance is reduced from $2^{2(n-1)}$*C of the monotonic switching in [6] to $2^{(n-1)}$*C, which is $2^{(n-1)}$ times better efficient. For example, in the case of the 10-bit SAR ADC, with the second reference voltage of Vref/32, the total capacitance of CDAC is reduced by 32 times compared to the conventional switching scheme [5]. Then, since we utilize the unit capacitance of 2fF in the CDAC, the

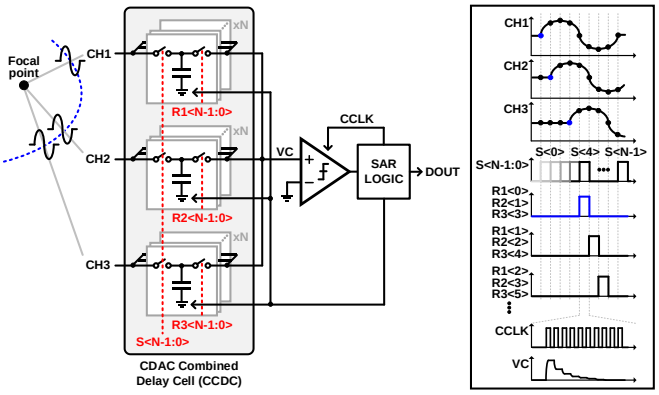

Fig. 2 *Sub-array beamforming SAR ADC with its timing diagram*

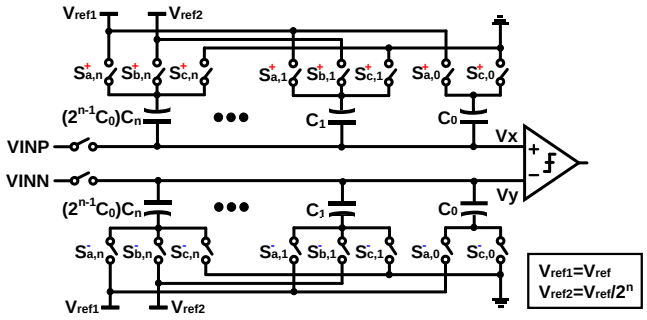

Fig. 3 *(2n)-bit binary weighted CDAC with a dual reference switching*

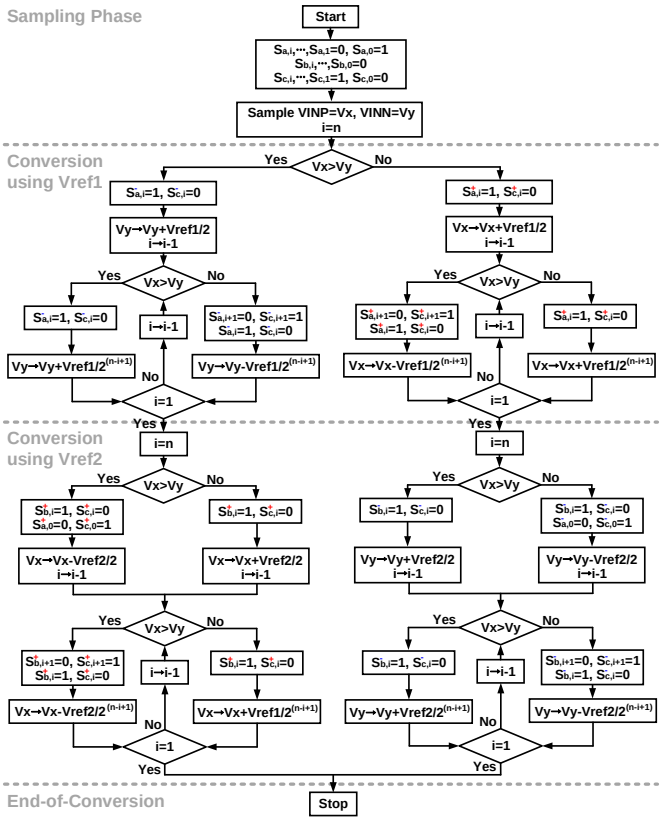

Fig. 4 *Switching flow diagram of CDAC using dual reference voltages*

capacitance of 64fF (32*C) can also be efficiently exploited in a unit delay cell, which occupies less area than even in the single delay cell of the previous works (single delay capacitance of 100fF in [2]).

Fig. 4 shows the switching flow diagram of a (2n)-bit SAR ADC using a dual reference switching scheme which is divided into sampling, MSB conversion using Vref1, and LSB conversion using Vref2 phases. In the sampling phase, the bottom plate of C0 is connected to the Vref1 while the other capacitors are connected to the GND by turning on the switches of Sa,0 and Sc,n,…, Sc,0. Then the VINP and VINN are sampled at the Vx and Vy nodes. Next, Vx and Vy are compared in the MSB conversion phase to connect the bottom plate of the MSB capacitor (Cn) to Vref1. For example, if Vx>Vy, Sa,n, and Sc,n on the Vy node are on and off, respectively, changing Vy into Vy+(Vref1)/2 while the switches on the Vx node remain still until the end of the MSB conversion phase. Then, if Vy+(Vref1)/2 < Vx, Sa,n-1 and Sc,n-1 of the Vy node are on and off, respectively, changing Vy+(Vref1)/2 to Vy+(Vref1)/4, otherwise (Vy+(Vref1)/2 > Vx), Sa,n and Sc,n are turned off and on, respectively, moving Vy+(Vref1)/2 to Vy-(Vref1)/4. After the switching flow completes the n-bit MSB conversion, the remaining n-bit conversion starts in the LSB conversion phase. The remaining switches on Vx nodes connect the bottom plate of C0 to the Vref2 in the same switching scheme as in the previous phase by turning on and off the Sb switches. Fig. 5 shows the operation example of 4-bit dual reference voltage SAR ADC based on the flow chart of Fig. 4.

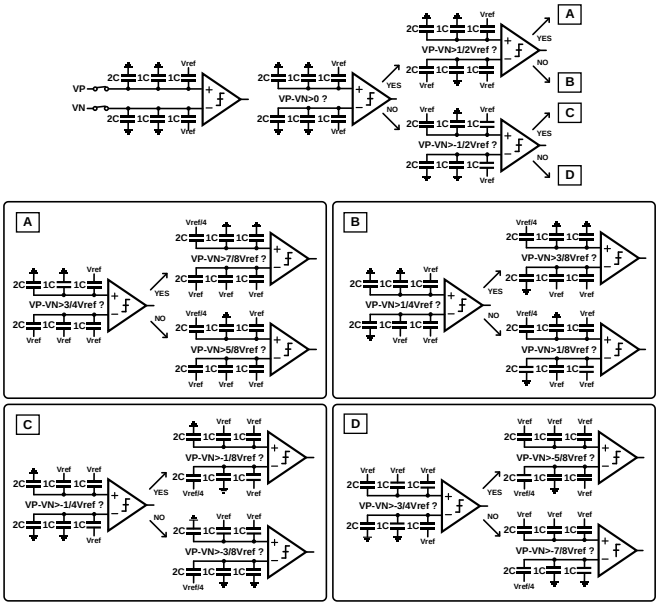

Fig. 5 *Proposed 4-bit switching procedure*

On top of the area efficiency of the dual reference CDAC, the CV^2 switching energy is also significantly reduced due to the 16*C MSB capacitance of the 10-bit SAR ADC. Table 1 compares the area and average switching-energy efficiency with previous low-energy 10-bit SAR ADCs. Due to the least total capacitance of 32*C, the size and energy efficiencies of CDAC are improved by 97.9% and 98.3%, respectively.

Implementation Results: Figure 6 shows beamforming ADC simulation results for a sub-array of 3 channels with a delay profile of 0, 1, and 3 unit delays in each channel. The unit delay is 16.67ns with a switching clock for delay cells and ADC sampling frequency of 60MHz. The number of delay cells (N) is 12, corresponding to an analog beamformer's maximum delay range up to 183.33ns. The carrier frequency of input signals is 7.5MHz, and 50mVpp amplitude is applied to the beamforming ADC. The delayed and accumulated signal through the CCDC structure is digitized by the dual reference SAR, displaying 47.46mVpp beamformed output waveform by 10-bit DAC. Table 2 compares the performance of sub-array beamforming RX with other beamformers for 3-D ultrasound imaging systems applications. Thanks to the CCDC structure with the dual reference SAR ADC, we achieve the total capacitance reduction in the delay cells and CDAC of the SAR ADC, which is down to N*64C per channel, minimizing area consumption. With the 2fF of C, the 64C is comparable to the capacitance of the single unit delay cell. Without the ADC buffer and reduced switching power in the SAR ADC, the beamforming ADC consumes 0.23mW per channel with a sampling rate of 60MHz for high spatial resolution. The performance characteristics indicate increased efficiency in the area, and power is achieved compared to the state-of-the-art works. The results also show the promising applicability of the proposed scheme in the miniaturized implantable devices for high-resolution imaging integrated with the small pitched transducer arrays.

Table1: Comparison of switching schemes for 10-bit SAR ADC

Switching method	Total Capacitance	Area savings (%)	Energy savings (%)
Conventional[5]	1024C	0	0
Monotonic[6]	512C	50	81.2
Bi-directional[7]	256C	75	82.8
Complex one-side[8]	256C	75	98.1
This work	32C	96.875	98.3

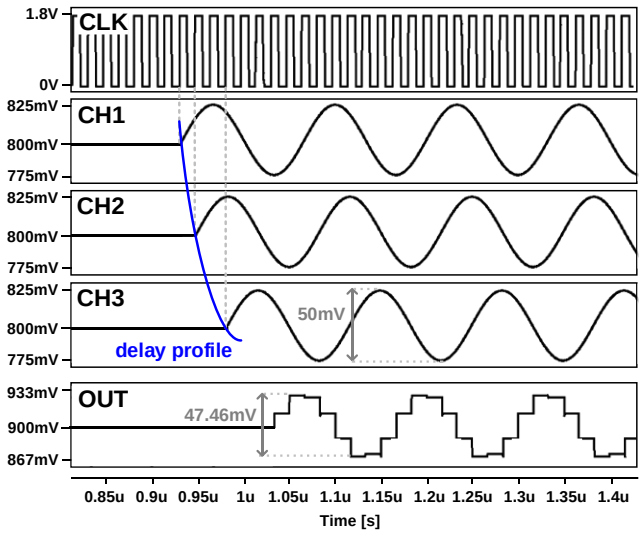

Fig. 6 *Beamforming simulation waveforms*

Conclusions: The CCDC structure shares the delay cells with the CDAC for the area and power-efficient analog sub-array beamforming ADC. The charge sharing of the delay cells removes the use of the ADC buffer, and the dual reference switching scheme in the ADC minimizes the capacitance of the CDAC, achieving 98.3% energy saving and 96.9% area saving compared to the conventional architecture. The beamforming ADC is designed with a 0.18µm CMOS process, consuming 0.23mW per channel. Correspondingly, this study shows its feasibility in the area and power efficient in-probe digitization for the next generation 3-d imaging systems with small pitched transducer arrays.

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Table2: Comparison of sub-array beamformer

	Ref.[1]	Ref.[2]	Ref.[3]**	Ref.[4]	This work
Technology	0.18 µm CMOS	0.13µm CMOS	0.18µm BCD	0.18µm CMOS	0.18µm CMOS
Center frequency	5MHz	3MHz	10MHz	5MHz	7.5MHz
Sub-array size (M)	1	8	4	9	3
No. of delay cells (N)	8	30	4	9	12
Total capacitance per channel	N·Cs +204.3C	(N+8)·Cs +2048C*	(N+2)·Cs	N·Cs +1024C	N·64C
ADC sampling frequency	20MHz	20-40MHz	No ADC	30MHz	60MHz
Beamformer power per channel***	0.85mW	99mW	0.33mW	0.17mW	0.23mW

* Assuming conventional SAR ADC

** ADC not implemented

*** LNA excluded for the comparison