On the design considerations of solid-state power amplifiers for satellite communications: a systems perspective

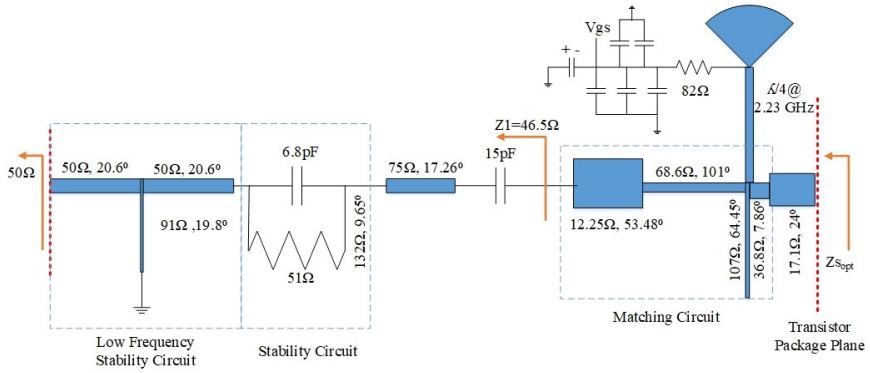
Rasit Tutgun[1], Emrah Öncü[2], and Emre Aktas[3]

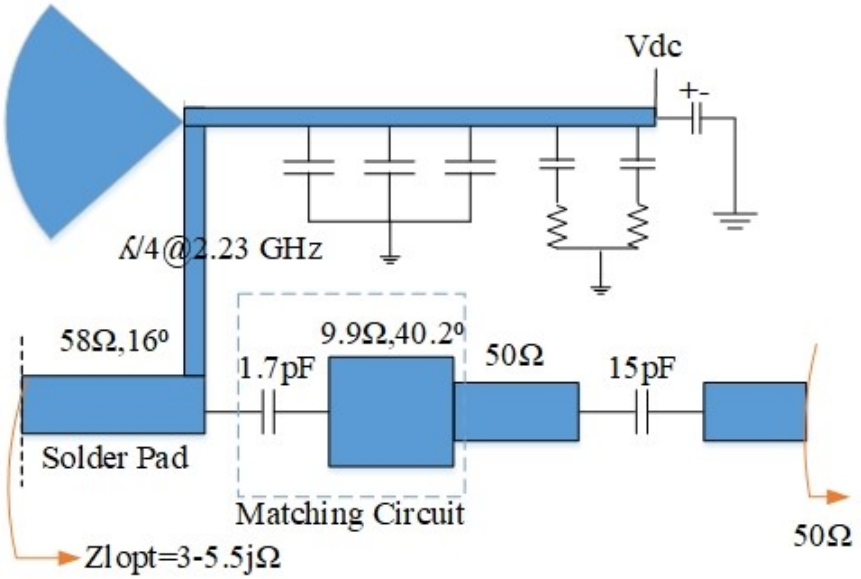
[1]Hacettepe Teknokent AS
[2]TUBITAK Uzay Teknolojileri Arastirma Enstitusu
[3]Hacettepe Universitesi

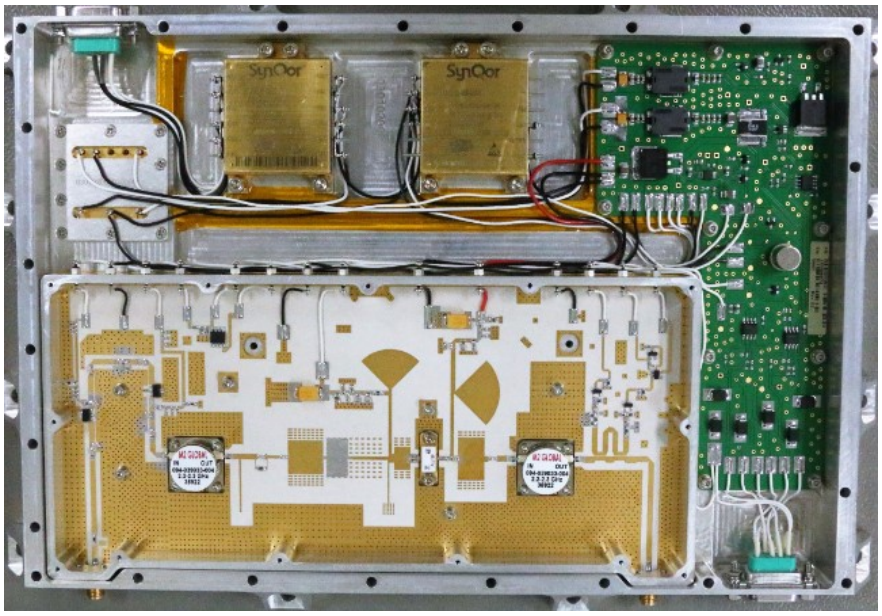
December 8, 2022

Abstract

Conventional solid-state power amplifier (SSPA) design approach isolates RF design from communication theory. In this paper, a unified SSPA design approach is proposed which optimizes SSPA parameters (bias voltage and input RF signal power) to minimize total DC power consumption while satisfying received SNR constraint specified by the link budget. The effect of SSPA nonlinearity is quantified by the error vector magnitude measured at its output and the corresponding received SNR degradation is analyzed. Using the quantitative metrics for received SNR, it is possible to evaluate highly nonlinear SSPA classes such as Class-B or deep-Class AB which are normally not considered in conventional SSPA design approach to be used in satellite communication applications.







Received: Added at production | Revised: Added at production | Accepted: Added at production

DOI: xxx/xxxx

ARTICLE TYPE

On the design considerations of solid-state power amplifiers for satellite communications: a systems perspective

Emrah Öncü[1] | Rasit Tutgun*[2] | Emre Aktas[3]

[1]TÜBİTAK UZAY, ODTÜ Kampüsü 06800 Ankara, Turkey
[2]Esen Sistem Entegrasyon, Hacettepe Teknokent 06800 Ankara, Turkey
[3]Hacettepe University, Beytepe Kampüsü 06800 Ankara, Turkey

Correspondence
*Rasit Tutgun, Hacettepe Teknokent 6F Blok No: 6 06800 Ankara Turkey. Email: rasit.tutgun@esensi.com.tr

Summary

Conventional solid-state power amplifier (SSPA) design approach isolates RF design from communication theory. In this paper, a unified SSPA design approach is proposed which optimizes SSPA parameters (bias voltage and input RF signal power) to minimize total DC power consumption while satisfying received SNR constraint specified by the link budget. The effect of SSPA nonlinearity is quantified by the error vector magnitude measured at its output and the corresponding received SNR degradation is analyzed. Using the quantitative metrics for received SNR, it is possible to evaluate highly nonlinear SSPA classes such as Class-B or deep-Class AB which are normally not considered in conventional SSPA design approach to be used in satellite communication applications.

KEYWORDS:
efficiency, error vector magnitude, linearity, satellite communications, solid-state power amplifier

1 | INTRODUCTION

Solid-state power amplifier (SSPA) is one of the most important components in a satellite communication transmit chain. It amplifies the RF signal right before the transmit antenna so that desired transmit power levels can be achieved in order to satisfy link quality. As the RF output power of the SSPA increases, the DC power consumption increases proportionally. However, DC power is a limited and expensive source in a satellite, and SSPA is one of the most DC power hungry components. Therefore, improving efficiency becomes critical for SSPA to reduce the DC power consumption. Typically, an SSPA is most power efficient near its saturation point. However, working near saturation almost always comes at a price of reduced linearity. The conventional communication system theory typically assumes linearity of all components in the transmitter and the receiver, including the SSPA at the transmitter. Thus, there is a fundamental trade-off between efficiency and linearity of SSPA circuit.

There is a considerable amount of work in the literature regarding the modeling of the SSPA nonlinearity and identifying the impact of the nonlinearity [1,2,3,4,5,6,7,8,9,10]. The level of nonlinearity is conventionally quantified by two parameters: error vector magnitude (EVM) and adjacent channel power ratio (ACPR). SSPA designers also utilize two-tone test and measure third and fifth order intermodulation distortions (IMD3 and IMD5) to characterize nonlinearity of the SSPA.

The conventional approach to SSPA design mainly focuses on maximizing the efficiency while staying in acceptable IMD and ACPR levels, given a desired output power level. The output power level is determined by link budget analysis. The link budget analysis is a crude method of determining the power levels and losses in a communication system, approximating each effect in the system as an additive term in dB scale. The EVM due to SSPA nonlinearity is simply accounted for as a constant term with some safety margins in this analysis.

Thus, the conventional approach to SSPA design decouples the microwave theory and the communication theory aspects of the design. The RF design is done decoupled from the communication system parameters such as SNR and symbol error rate

at the receiver, aiming solely to improve the power efficiency while roughly limiting the nonlinearity using the EVM, ACPR, IMD parameters. The communication theory simply tells the RF designer the desired output power level. The SSPA designer then selects from off-the-shelf SSPA units considering output power and IMD levels. This approach does not allow taking into account the interactions between microwave design parameters and the overall link SNR. Most contemporary RF transistor and SSPA manufacturers do not even provide complete EVM specifications, showing the gap between microwave design and communication system design. In this paper, we propose a unified design approach for the SSPA introduced in [11]. This approach combines the received SNR requirements with SSPA design parameters, namely the transistor bias voltages and the input RF power. We recognize that the overall goal is to satisfy the received SNR level while minimizing the power consumption of the SSPA. Therefore, we set up the design problem in this manner, without identifying output power level and efficiency of the SSPA, which we consider as intermediate parameters used to separate the microwave power amplifier theory and communication theory aspects of the design. We consider the overall SNR at the receiver, including the EVM produced by the SSPA. By combining RF design and communication theoretical aspects, we show that lower power consumption levels for the SSPA can be achieved, compared to the conventional approach. Moreover, we show that the typical SSPA design approaches may not be optimal in the sense of minimizing the power consumption.

The rest of the paper is organized as follows. In Section 2, the problem definition is given where the conventional SSPA design approach is briefly explained. In Section 3, the proposed SSPA design approach is discussed. In Section 4, an S-Band SSPA is designed for a satellite transmitter as a case study. In this section, a step-by-step procedure is followed starting from the communication link design to specify the SSPA parameters. Section 5 concludes the paper.

2 | PROBLEM DEFINITION

The first step of the unified SSPA design approach is to define the effects of power amplifier on the system technical budgets such as link budget and power budget. The most critical SSPA parameter is RF output power (P_{out}) which is directly related to these budgets, namely:

$$SNR_r = f_1(P_{out}) \tag{1}$$

$$P_{dc} = f_2(P_{out}) \tag{2}$$

where the first equation is the link budget with the figure of merit received SNR (SNR_r). The second equation is the power budget of SSPA where P_{dc} is the DC power consumption of the amplifier. The first functional relationship is found using the well-known Friis Transmission Equation:

$$SNR_r = \frac{P_r}{N} = \frac{P_{out} \times G_t \times G_r}{L \times N} \tag{3}$$

where P_r is received power at the receiver, G_t is transmit antenna gain, G_r is receive antenna gain, L is total signal loss between the transmitter and the receiver, and N is total noise power at the receiver.

Signal loss (L) depends on free-space loss and atmospheric losses. For the sake of simplicity, we take this parameter as constant for the rest of the paper. Total noise power (N) at the receiver is assumed to be dependent only on the receiver thermal noise and radiated bodies in the field of view of receive antenna. This assumption is valid for the ideal transmitter case where transmitter does not contribute to the noise at the receiver. Nevertheless, this will not be the case when transmitter is nonlinear because transmitter itself corrupts the signal at its output and causes degradation in the received SNR. The amount of degradation is characterized by noise contribution of the transmitter at the receiver:

$$N = N_d + N_r \tag{4}$$

N_r is the receiver thermal noise and N_d is the total amount of noise caused by the nonlinear distortion of SSPA. N_d is directly related to the linearity of SSPA and power amplifier class which is determined by the bias voltages (V_{gs}, V_{ds}) as well as output and input RF power (P_{out}, P_{in}):

$$N_d = g_1(P_{out}, P_{in}, V_{gs}, V_{ds}) \tag{5}$$

We will later describe the nonlinear characteristics of power amplifier classes and the relation given in Equation (5) in Section 3. We also calculate the amount of SNR degradation in Section 4 for a given scenario.

The second relationship between P_{out} and P_{dc} is more complicated where power consumption of an SSPA is related to the choice of power amplifier class. We denote this relationship with the implicit formula given below:

$$P_{dc} = g_2(P_{out}, P_{in}, V_{gs}, V_{ds}) \tag{6}$$

In general, the expressions in (5) and (6) are hard to formulate explicitly, but they can be obtained via measurements for various input parameters. We tabulate our results based on the measurements of a device under test in Section 4.

General practice teaches us that N_d in (5), in other words the signal corruption, tends to increase with the use of nonlinear power amplifiers compared to linear amplifiers. This is opposite for P_{dc} in (6); nonlinear PAs have better power efficiency than linear amplifiers for a specific output power. Thus, there is a trade-off between linearization and efficiency. The proposed approach in this paper aims to find the optimum point of this trade-off with a unified view: minimize (2) while keeping (1) above a desired level, utilizing the measurement based enumerations of the relationships in (5) and (6). Before describing this design approach in Section 3, we provide an overview of conventional approach in the following subsection, in order to lay a foundation and help highlight the novelty of our approach.

2.1 | Conventional SSPA Design Method

The first step of a communication system design is doing link budget calculations and transmitter system design. For a given data rate, BER, link margin constraint, the designer determines the modulation and coding scheme, and this step provides the necessary transmitter parameter of EIRP (equivalent isotopically radiated power). After link budget is done, the transmitter system design parameters of antenna gain and output power are specified. At the second step, the survey of commercially available RF transistors is done to fulfill the gain and power requirements of the SSPA, and a suitable RF transistor is selected. The third step is designing the SSPA circuit. However, at this point, PA designer has almost no information about the end to end communication link. This may force them to stay in the safest side and choose Class A mode when the linearity is considered. This results in a low efficiency, and hence DC power consumption will be high. In order to increase the efficiency, PA designer should decrease the conduction angle of the transistor, but this will degrade the linearity of the SSPA and it is obvious that this becomes a hard decision to be made. So, without having a clear idea about the end to end communication quality, the logical starting point tends to become choosing mid-class AB mode which seems like an effective bias point when efficiency and linearity are considered. Once this decision is made, the following design steps are all in the RF domain and the design activities and issues are carried out by RF/microwave engineering viewpoint.

3 | PROPOSED UNIFIED SSPA DESIGN METHOD

In the proposed unified SSPA design method, the first two steps are the same as in the conventional method. The third step is the preliminary design phase in which the SSPA designer determines several (V_{gs}, P_{in}) pairs that bias the transistor from Class A mode to Class B mode. In each mode, the optimum load values to have the maximum output power from the transistor might change. So, designer measures, calculates or simulates the transistor to find the load-pull contours for all (V_{gs}, P_{in}) pairs. By using the load-pull contours and S-parameters for each pair, input/output matching circuits and bias networks are designed. At the end of this step, there may be several prototype SSPA circuits which are ready to be tested. In the fourth step, prototype SSPA circuits for each pair are tested with the modulated signal, and the following parameters are measured: EVM, DC current and RF output power. Utilizing these measurements, the relationships in (5) and (6) are obtained. After that, the DC power consumptions and the received SNR values in (1) and (2) can be calculated for each bias pair. These calculations are explained in the following.

Received SNR is degraded due to the EVM caused by SSPA nonlinearity. We know that EVM is inversely proportional to the square root of SNR [12]:

$$EVM = \frac{1}{\sqrt{SNR}} \tag{7}$$

By using this fact, we can now formulate the effect of EVM, measured by the signal analyzer, on the received SNR measured at the receiver. Measured EVM from the signal analyzer contains noise from signal analyzer, as well as the nonlinear effects of the SSPA. The SNR at the signal analyzer (SNR_{sa}) can be written as

$$SNR_{sa} = \frac{\alpha P_{out}}{\alpha N_d + N_{sa}} \tag{8}$$

where P_{out} is the RF output power of PA, α is the attenuation between SSPA output and signal analyzer input, N_d is the power of additive noise caused by nonlinear distortion of SSPA, and N_{sa} is the amount of noise caused by signal analyzer. We assume that the noise components are independent of each other, hence they can be added directly. In light of (7), we can now rearrange

the above equation in terms of EVM as below:

$$EVM_m^2 = \frac{1}{SNR_{sa}} = \underbrace{\frac{N_d}{P_{out}}}_{EVM_d^2} + \underbrace{\frac{N_{sa}}{\alpha P_{out}}}_{EVM_{sa}^2} \tag{9}$$

EVM_m is measured by the signal analyzer and composed of EVM_d, which is caused by the nonlinear distortion of SSPA, and EVM_{sa}, which is due to the signal analyzer itself. In order to measure EVM_{sa}, we make measurements in the low P_{out} region first. We assume that for low P_{out} (linear region of SSPA), nonlinear distortion from SSPA is negligible, hence $EVM_d = 0$ and $EVM_m = EVM_{sa}$. So, we can find EVM_{sa}, and separate the effects of signal analyzer from SSPA.

We can now use the same methodology for the calculation of received SNR (SNR_r) under the effect of nonlinear distortion of SSPA. Like the SNR formula above, it is possible to write received SNR in terms of noise from nonlinear distortion (N_d) and receiver thermal noise (N_r):

$$SNR_r = \frac{\beta P_{out}}{\beta N_d + N_r} \tag{10}$$

Now, β represents all the gains and losses between the transmitter and the receiver including free-space loss, atmospheric losses, transmit and receive antenna gains. Received SNR can be expressed in terms of ideal SNR (SNR_i), which is calculated at the very first step of system design with the assumption of distortion free SSPA, and the EVM of SSPA (EVM_d), which is characterized using the procedure explained above:

$$\frac{1}{SNR_r} = \frac{1}{SNR_i} + EVM_d^2 \tag{11}$$

The expression above tells us that ideal SNR is degraded with nonlinear distortion and the amount of degradation can now be calculated. Second statement is that the amount of SNR degradation is increasing while ideal SNR is increasing. This is because the total amount of noise at the receiver is dominated by the noise from the nonlinear distortion of SSPA.

Following the calculation of received SNR, preliminary link budget at the first step shall be updated to include the effect of PA distortion. As a reminder, in the third step several prototype SSPA circuits have been determined as a candidate of final design. At this stage, these candidates are evaluated in terms of final received SNR performance using an optimization procedure described below:

$$\begin{aligned} (V_{gs}, P_{in})_{optimum} &= \min_{V_{gs}, P_{in}} P_{dc} \\ &\text{s.t. } SNR_r \geq SNR_{req} \end{aligned} \tag{12}$$

This optimization problem tells us that optimum SSPA design is determined by (V_{gs}, P_{in}) pair which minimizes DC power consumption of SSPA (P_{dc}) while satisfying the minimum SNR requirement ($SNR_r \geq SNR_{req}$) in order to ensure link quality. The proposed unified SSPA design method, contrary to the conventional approach, enables SSPA designer to optimize power amplifier parameters with respect to system level metrics such as total power consumption and overall link quality.

4 | CASE STUDY: A UNIFIED SSPA DESIGN FOR A SATELLITE TRANSMITTER

In this section, an example SSPA design based on [11] for a satellite transmitter will be explained following the proposed procedure explained in Section 3.

4.1 | Step 1: Link Budget Calculation and Transmitter System Design

Starting point of system design is link budget calculation for a satellite communication scenario. We consider a LEO satellite orbiting at a sun synchronous orbit with an altitude of 700 km above the earth surface. The worst case for the communication link is the farthest distance between the satellite and the earth station. Generally, an elevation of 5 degree from the horizon of the earth station is assumed to be the edge of communication cone. This makes the longest distance 2517.47 km and free-space loss is calculated as $L = 168.12$ dB for the carrier frequency given below including atmospheric losses. For this point-to-point link, the communication requirements are defined as below:

- **Transmitted signal:** Carrier frequency 2.23 GHz, Uncoded QPSK, baud rate of 2 MHz, transmit filter root-raised cosine (RRC) with roll-off 0.65.

- **Maximum BER:** 10^{-7} (Minimum required SNR is $SNR_{req} = 14.2dB$ with a 3 dB margin).
- **Earth station parameters:** Earth station receiver parameter is calculated as $G_r/T = 17.87$ dB/K.

Based on the communication requirements listed above, minimum EIRP is found to be 1 W or 30 dBm. To satisfy a minimum EIRP of 30 dBm with an antenna gain of 0 dBi and 7 dB post-SSPA losses, the minimum RF output power of SSPA shall be at least 37 dBm.

Next step is to determine the overall gain of transmitter from the output of the modulator to the output of the SSPA. Usually modulator integrated circuit is selected first, and the rest of the chain is determined accordingly. We assume an output power of 0 dBm for the modulator. Hence the necessary power gain of SSPA is specified as 37 dB. This is the end of first step. In the next step, SSPA topology and requirements of the final amplification stage will be derived.

4.2 | Step 2: RF Transistor Survey for SSPA and Determine SSPA Topology

In the previous step, output power and overall gain requirements of the SSPA are derived based on the link budget calculations. According to the analysis, the SSPA shall satisfy minimum RF output power of 37 dBm and minimum small signal gain of 37 dB. For the specified carrier frequency (S-Band), RF power transistors typically have a small-signal gain of 7 dB to 12 dB. After a survey of suitable RF transistors for this circuit, we have chosen FLL120MK, an unmatched Gas FET from SEDI, which has the typical P_{1dB} of 40 dBm and the typical linear gain of 11 dB, because of its space heritage in BİLSAT[13], RASAT[14] and GÖKTÜRK-2[15] low-earth orbit satellites of TÜBİTAK UZAY. The remaining necessary gain (28 dB) will be allocated between the driver amplifier and the pre-driver stages. The other initial requirements for SSPA design are derived from the common engineering practice: $S_{11} < -15$ dB, $S_{22} < -10$ dB.

4.3 | Step 3: Preliminary SSPA Design (For All V_{gs} and P_{in})

After analyzing transistor's DC current-voltage curve, pinch-off voltage and saturated drain current (I_{dss}) values were specified as -2.25 V and 4.68 A, respectively. When drain to source voltage (V_{ds}) was 10 V and gate to source voltage (V_{gs}) was -1.4 V, drain to source current (I_{ds}) was measured as 2.34 A, which is half of the I_{dss} value. Since there was no possibility for us to observe the current and voltage waveforms at the device plane, it was concluded that (-1.4 V, 10 V) bias voltage pair could be taken as Class A bias condition. As a result, there is a V_{gs} range from -1.4 V to 2.25 V to decide an optimum operating point which can satisfy the requirements given for the amplifier circuit. After these measurements, load-pull contours are plotted under $V_{ds} = 10$ V for the following (V_{gs}, P_{in}) pairs:

$$(V_{gs}, P_{in}) = (-1.4 : 0.1 : -2 \text{ V}, 24 : 0.5 : 29 \text{ dBm}) \tag{13}$$

When $V_{gs} = -2$ V, I_{dq} is observed to be 5% of the I_{dss}. By examining the load-pull contours for $P_{out} = 37.5$ dBm (0.5 dB margin is added to compensate the isolator losses), an optimum load impedance region which is the intersection of all suitable (V_{gs}, P_{in}) pairs is found as $Z_{opt} = 3 - 5.5j$. So, only one output matching circuit is designed to transform 50 Ω system impedance to $(3 - 5.5j)$ Ω at the transistor's package plane. After that, optimum source impedance is found for the specified power gain while transistor output sees the optimum load impedance.

Input circuit consists of impedance matching and stability networks, bias circuit and a DC blocking capacitor. According to source-pull contours for specified gain of 11 dB, real part of the optimum source impedance (Z_{sopt}) varies between 1.6 Ω and 3.4 Ω, imaginary part of Z_{sopt} varies between $-4.5j$ Ω and $-7.6j$ Ω. In order to stay away from the boundary of the chosen impedance contour, Z_{sopt} was specified as $2.5 - 6.05j$ at 2.23 GHz. After specifying the optimum source impedance, stability of the transistor under the operating DC point for 0.1 MHz to 5 GHz frequency range was analyzed. For frequencies below 1366 MHz, stability factor K was lower than 1 and maximum available gain was higher than 22 dB. To make the transistor unconditionally stable, a stability network with lumped components and transmission lines was designed. A high Q capacitor was connected in parallel with 51 Ω RF resistor with very thin transmission lines to reduce out of band gain with minimal in-band loss. A short circuit stub was cascaded in order to increase the gain reduction below 450 MHz while presenting high impedance above 2 GHz. An electrically short 75 Ω transmission line and a 15 pF DC blocking capacitor were placed to resonate the reactive part of the input impedance at the operating frequency. Hence, $Z_1 = 46.5$ Ω at 2.23 GHz. A 4-pole lumped low-pass impedance matching circuit was synthesized to convert Z_1 to Z_{sopt}. Then, each lumped component was transformed into distributed elements to minimize the insertion loss. Before optimizing the matching circuit, gate bias circuit was designed. This

circuit consists of a radial stub with a narrow $\lambda/4$ transmission line to present a high impedance at 2.23 GHz, by-pass capacitors and a series resistor to enhance low frequency stability. Impedance matching and bias circuits were then optimized together. Input circuit is shown in Fig. 1.

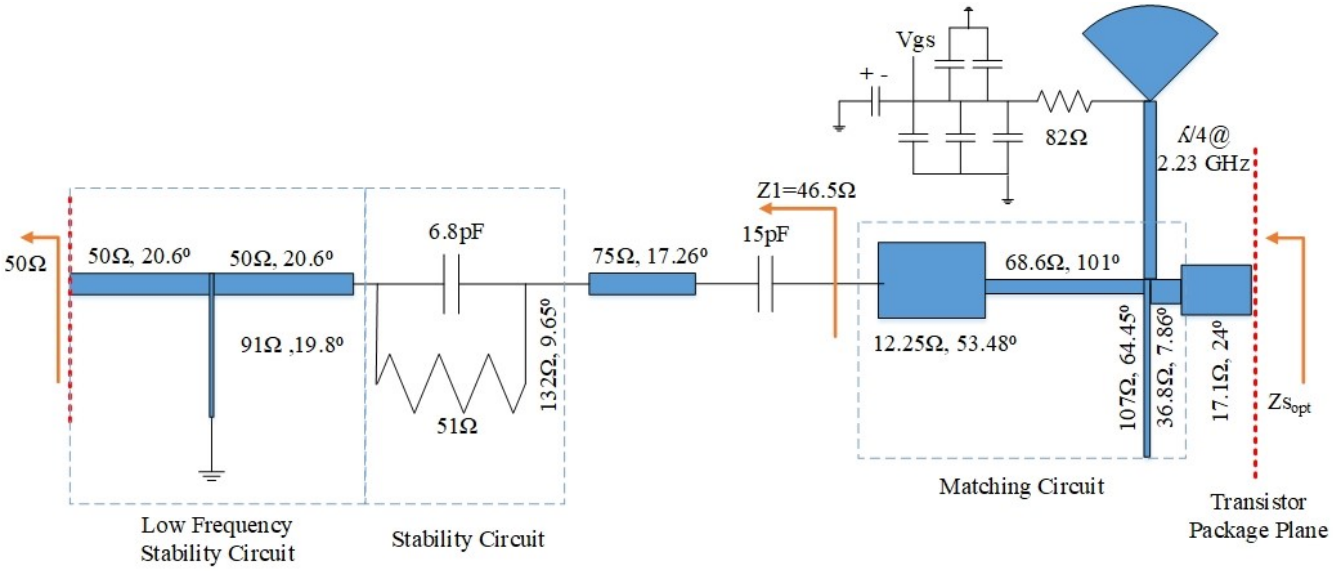


Figure 1 Schematic of the input circuit

A simple low-pass matching circuit was designed to transform 50 Ω system impedance to optimum load impedance. It was observed that transistor's output soldering pad transforms the optimum load in the wrong direction, so series inductor was replaced with a series capacitor in the matching circuit. Bias circuit consists of radial stub and a high impedance quarter-wave line with by-pass capacitors. Output matching and bias circuits were then optimized together. Output circuit is shown in Fig. 2. The measurement results will be discussed in the next step.

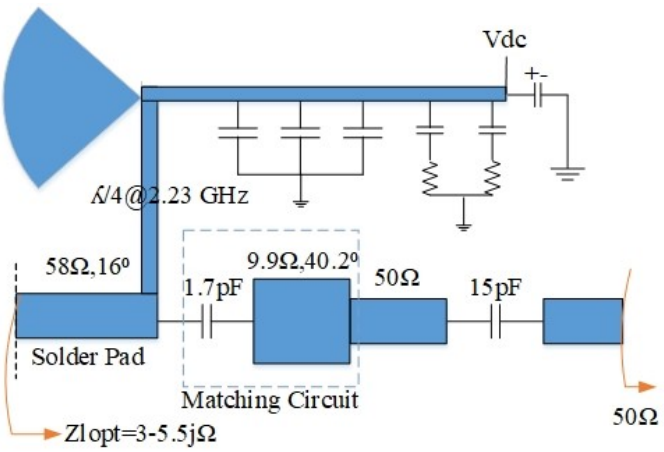


Figure 2 Schematic of the output circuit

4.4 | Step 4: Measure EVM and I_{dc}, Calculate SNR_r and P_{dc} (For All V_{gs} and P_{in})

The parameters P_{out}, EVM and I_{dc} of the prototype circuit are measured. The channel power of this signal (P_{in}) is varied from 24 dBm to 29 dBm with 0.5 dB steps. Bias voltages, V_{ds} is constant at 10 V and V_{gs} is varied from -1.4 V to -2 V with 0.1 V steps. Measurement (EVM and P_{out}) and analysis (P_{dc} and SNR_r) results are shown in Table 1 and Table 2, respectively.

Table 1 Measurement results

	P_{out} (dBm)						
	$V_{gs}(V)$						
P_{in} (dBm)	−1.4	−1.5	−1.6	−1.7	−1.8	−1.9	−2.0
24.0	34.08	34.06	34.05	34.06	34.05	34.15	34.11
24.5	34.53	34.61	34.66	34.71	34.81	34.89	34.96
25.0	35.08	35.06	35.06	35.08	35.09	35.19	35.17
25.5	35.54	35.60	35.66	35.72	35.82	35.89	35.98
26.0	36.04	36.02	36.02	36.06	36.08	36.17	36.17
26.5	36.43	36.47	36.53	36.60	36.69	36.73	36.82
27.0	36.80	36.79	36.81	36.83	36.87	36.94	36.95
27.5	37.10	37.17	37.22	37.26	37.30	37.32	37.40
28.0	37.41	37.39	37.40	37.40	37.45	37.47	37.48
28.5	37.62	37.68	37.70	37.72	37.73	37.73	37.75
29.0	37.84	37.80	37.81	37.78	37.82	37.84	37.83
	EVM (%)						
	$V_{gs}(V)$						
P_{in} (dBm)	−1.4	−1.5	−1.6	−1.7	−1.8	−1.9	−2.0
24.0	1.10	0.90	0.70	0.45	0.58	0.80	1.05
24.5	1.40	1.20	0.90	0.75	0.78	1.05	1.25
25.0	1.90	1.60	1.20	1.10	1.25	1.45	1.60
25.5	2.30	1.90	1.60	1.60	1.79	1.95	2.10
26.0	2.70	2.30	2.10	2.10	2.25	2.50	2.70
26.5	2.90	2.65	2.50	2.60	2.70	3.00	3.10
27.0	3.00	3.00	2.90	3.10	3.20	3.30	3.60
27.5	3.50	3.40	3.30	3.50	3.60	3.65	3.80
28.0	4.40	4.50	4.30	4.20	4.00	4.10	4.20
28.5	6.10	6.00	5.60	5.20	5.00	5.00	4.80
29.0	7.40	7.50	7.00	6.50	6.10	6.00	5.60

4.5 | Step 5: Optimization

Optimization procedure, defined in (12), is simply searching for the (V_{gs}, P_{in}) pair which minimizes P_{dc} and also results received SNR (SNR_r) satisfying the SNR requirement given in Step 1 (which is 14.2 dB) among the Table 1 and Table 2 where acceptable solutions satisfying SNR requirement is shown with underlined cells. If the SNR constraint is changed, acceptable region in the table for optimum pair search shall be updated. Optimization results are listed in Table 3. As a comparison, conventional Class A and mid-Class AB results are also given (with red highlighted cells in the underlined records). These results show that the optimum solution is a deep-Class AB power amplifier. In terms of power efficiency, deep-Class AB is expected to be the one of the best solutions but traditional approach does not consider utilizing this amplifier because it is assumed to be highly nonlinear.

Table 2 Analysis results

	P_{dc} (W)						
	$V_{gs}(V)$						
P_{in} (dBm)	−1.4	−1.5	−1.6	−1.7	−1.8	−1.9	−2.0
24.0	13.80	11.80	10.20	8.80	8.00	7.50	7.20
24.5	13.80	12.00	10.30	9.20	8.50	8.20	7.90
25.0	13.90	12.00	10.60	9.30	8.70	8.30	8.10
25.5	13.90	12.20	10.70	9.80	9.30	9.00	8.80
26.0	13.90	12.10	10.90	10.00	9.50	9.10	9.50
26.5	13.70	12.20	11.00	10.40	9.90	9.70	9.50
27.0	13.40	11.90	11.10	10.40	10.00	9.70	9.50
27.5	13.00	12.00	11.10	10.60	10.20	10.00	9.80
28.0	12.70	11.70	11.00	10.50	10.20	9.90	9.80
28.5	12.40	11.70	11.10	10.70	10.30	10.10	9.90
29.0	11.90	11.30	10.90	10.50	10.20	10.00	9.80
	SNR_r (dB)						
	$V_{gs}(V)$						
P_{in} (dBm)	−1.4	−1.5	−1.6	−1.7	−1.8	−1.9	−2.0
24.0	11.16	11.14	11.13	11.14	11.13	11.23	11.19
24.5	11.60	11.68	11.74	11.79	11.89	11.97	12.03
25.0	12.14	12.13	12.13	12.16	12.16	12.26	12.24
25.5	12.58	12.65	12.72	12.78	12.88	12.94	13.03
26.0	13.06	13.06	13.06	13.10	13.12	13.20	13.19
26.5	13.43	13.49	13.55	13.62	13.70	13.72	13.80
27.0	13.79	13.78	13.81	13.81	13.84	13.91	13.89
27.5	14.05	14.12	14.18	14.20	14.23	14.25	14.31
28.0	14.26	14.23	14.26	14.27	14.34	14.35	14.35
28.5	14.25	14.32	14.39	14.46	14.50	14.50	14.54
29.0	14.24	14.19	14.28	14.33	14.43	14.46	14.51

The proposed SSPA design approach reveals the true potential of deep-Class AB or even Class B for this communication scenario by calculating the received SNR. The optimized results lowers power consumption by 2.9 W (29.59%) compared to conventional Class A, and 0.7 W (7.14%) compared to conventional mid-Class AB with similar received SNR results.

4.6 | Step 6: Finalize SSPA Design

After determining the optimum (V_{gs}, P_{in}) pair, SSPA design is completed following the conventional design steps including adjusting bias voltages and tuning input/output matching circuits. Complete qualification model is shown in Fig 3.

5 | CONCLUSION

In this paper, a unified SSPA design approach is proposed and an example S-Band SSPA design for a satellite transmitter is realized following the proposed approach. The proposed unified SSPA design approach combines RF design and communication theoretical aspects by minimizing power consumption under a received SNR constraint originated from the link budget. The received SNR is degraded by the nonlinear distortion of SSPA and the amount of SNR degradation is calculated using the

Table 3 Optimization results

P_{in} (dBm)	V_{gs} (V)	SNR_r (dB)	P_{dc} (W)	Description
27.5	−2.0	14.31	9.8	Optimization result 1
28.0	−2.0	14.35	9.8	Optimization result 2
29.0	−2.0	14.46	9.8	Optimization result 3
28.0	−1.4	14.26	12.7	Conventional Class A
28.0	−1.7	14.27	10.5	Conventional Mid-Class AB

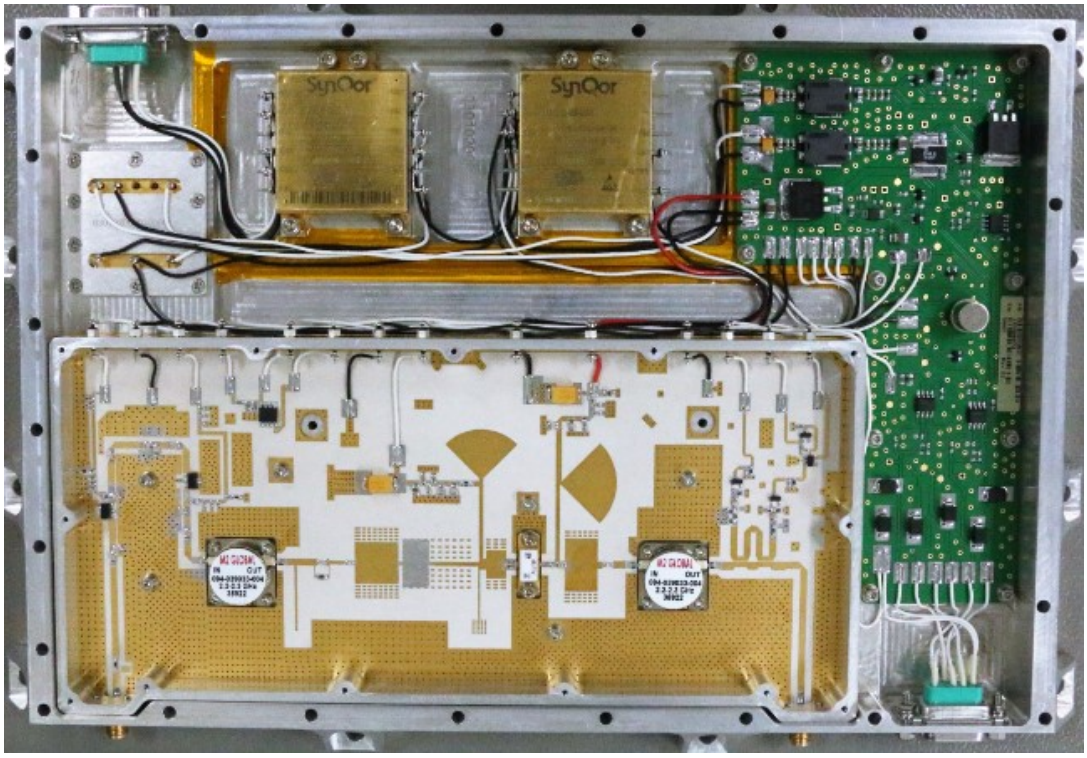


Figure 3 Qualification model of the SSPA

measured EVM. By following the proposed approach, it is possible to find a power amplifier solution which would not be considered in the conventional approach as it is highly nonlinear, but still achieves the desired received SNR with a lower required DC power. It is important to note that the obtained result will be valid only for a specified communication scenario. The proposed approach shall be repeated for every SSPA design under different modulation assumptions, especially high order modulations, and other semiconductor technologies such as Gallium-Nitride (GaN) which is left as a future work.

References

1. Zayani, R., Shaiek, H., Roviras, D.: Efficient precoding for massive MIMO downlink under PA nonlinearities. IEEE Commun. Lett. (2019). https://doi.org/10.1109/LCOMM.2019.2924001

2. Yoda, D., Ochiai, H.: Decision region optimization and metric-based compensation of memoryless nonlinearity for APSK systems. IEEE Trans. Broadcast. (2018). https://doi.org/10.1109/TBC.2017.2781128

3. Song, J., Ochiai, H.: Amplifier efficiency and distortion trade-off of OFDM system with iterative clipping and filtering. IEEE Wirel. Commun. Netw. Conf. WCNC (2014). https://doi.org/10.1109/WCNC.2014.6952157

4. Ochiai, H.: An analysis of band-limited communication systems from amplifier efficiency and distortion perspective. IEEE Trans. Commun. (2013). https://doi.org/10.1109/TCOMM.2013.020413.120384

5. Mollén, C., Larsson, E. G., Eriksson, T.: Waveforms for the massive MIMO downlink: Amplifier efficiency, distortion, and performance. IEEE Trans. Commun. (2016). https://doi.org/10.1109/TCOMM.2016.2557781

6. Moghadam, N. N., et al.: On the energy efficiency of MIMO hybrid beamforming for millimeter-wave systems with nonlinear power amplifiers. IEEE Trans. Wirel. Commun. (2018). https://doi.org/10.1109/TWC.2018.2865786

7. Gutman, I.: Impact of non-linear power amplifier on on digital communications, OFDM, single carrier. Dr. Philos. Thesis, Ben-Gurion Univ. Negev. (2013).

8. Gulgun, Z., Yilmaz, A. O.: Detection schemes for high order M-ary QAM under transmit nonlinearities. IEEE Trans. Commun. (2019). https://doi.org/10.1109/TCOMM.2019.2905569

9. Enzinger, H., Freiberger, K., Vogel, C.: A joint linearity-efficiency model of radio frequency power amplifiers. Proc. - IEEE Int. Symp. Circuits Syst. (2016). https://doi.org/10.1109/ISCAS.2016.7527225

10. Costa, E., Midrio, M., Pupolin, S.: Impact of amplifier nonlinearities on OFDM transmission system performance. IEEE Commun. Lett. (1999). https://doi.org/10.1109/4234.749355

11. Öncü, E., Tutgun, R., Kilic, H. D.: An S-Band solid-state power amplifier for low earth orbit satellite telemetry communications. IEEE Asia-Pacific Microwave Conference APMC (2020). https://doi.org/10.1109/APMC47863.2020.9331415

12. Shafik, R. A., Rahman, M. S., Islam, A. H. M. R.: On the extended relationships among EVM, BER and SNR as performance metrics. Proc. 4th Int. Conf. Electr. Comput. Eng. ICECE (2006). https://doi.org/10.1109/ICECE.2006.355657

13. Belce, O., Telli, A., Maynard, K.: BILSAT-1 communication subsystem. Proc. International Conference on Recent Advances in Space Technologies RAST (2003). https://doi.org/10.1109/RAST.2003.1303896

14. Icoz, D., et al.: Communication subsystem of RASAT. Proc. International Conference on Recent Advances in Space Technologies RAST (2011). https://doi.org/10.1109/RAST.2011.5966983

15. Gürgenburan, G., Cinar, E.: GÖKTÜRK-2: Two years of operation. Proc. International Conference on Recent Advances in Space Technologies RAST (2015). https://doi.org/10.1109/RAST.2015.7208378