Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ for Analog Memory and In-Memory Computing Applications down to Deep Cryogenic Temperatures

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Abstract

Low-power non-volatile memories operating down to deep cryogenic temperatures are important for a large spectrum of applications from high-performance computing and electronics interfacing quantum computing hardware to space-based electronics. Despite the potential of $Hf_{0.5}Zr_{0.5}O_2$ (HZO), thanks to its compatibility with complementary metal-oxide-semiconductor (CMOS) back-end-of-line processing, only few studies of HZO based memory devices down to cryogenic operation temperatures exist. Here, we report on analog ferroelectric memory stack fabrication with 10 nm HZO and its detailed characterization under a wide range of pulse amplitudes and frequencies from 300 K down to 4 K. When operated at temperatures below 100 K, HZO devices can support high amplitude voltage pulses, yielding record high remnant polarization P_r of up to 75μC cm^{-2} at ±7 V_p (14 V_{pp}) pulse amplitudes accompanied with frequency-dependent memory window between 6 and 8 V. Devices show excellent endurance exceeding 10^9 cycles of ±5 V_p (10 V_{pp}) and P_r of 30 μC cm^{-2} without significant degradation of coercive voltages or loss of polarization at cryogenic temperatures. At least 20 reproducible analog states for temperatures below 100 K with almost ideal linearity of intermediate polarization states in both pulse directions are observed, demonstrating the high potential of analog cryogenic ferroelectric memories, essential for online training in In-Memory-Computing architecture.

1. Introduction

Ferroelectric (FE) memory devices offer significant advantages in terms of energy-efficiency, fast operation, endurance and stable data retention over flash or other CMOS-compatible emerging memory technologies, like resistive random-access memories or phase-change memories. [1, 2] FE

random access memories (FeRAMs) with 1 transistor-1 capacitor (1T1C) structure where information is encoded through the FE polarization charges in the capacitor layer is currently the most matured ferroelectric memory technology. However, difficulty in scaling the capacitors beyond a certain limit and destructive readout makes FeRAMs unsuitable for dense integration and refresh-free operation. The next candidate from the technology maturity level is FE field-effect transistors (FeFETs), where the FE layer is integrated in the gate insulator stack of an FET. FeFETs can have a wide conductance window, endurance exceeding 10^6 cycles at room temperature, and high bit resolution - properties that are conducive for nonvolatile memories (NVM) operation and high-accuracy online learning in neuromorphic computing. [3, 4] To make FeFET technology commercially viable, scaling of the FE layer in both lateral and vertical dimension is needed. While most of the reported works on FE memories or commercially available FeRAM devices were based on oxide perovskite FE, [5, 6] incompatibility of oxide perovskites with standard CMOS fabrication processes makes their 3D-integration with readout and logic circuits difficult. Additionally, absence of ferroelectricity in ultrathin perovskite ferroelectrics made their scaling prospect limited. Discovery of ferroelectricity in doped HfO_2 system [7] renewed the interest in industrial scale FE memories that can be integrated with CMOS circuits either at front-end-of-line (FEOL) or back-end-of-line (BEOL). [8]

Today, the demand for energy-efficient memories operating down to cryogenic temperatures is becoming more important for many applications, *i.e.*, high-performance computing (HPC), storage-class memory in data centers, space technologies and quantum computing. "Cold-MRAM" [9] or "Cold-FeFETs" [10] which are based on devices with ferroic ordering of materials operated at low temperature (*i.e.*,77 K) are emerging as strong embedded memory technology candidates for augmenting volatile SRAM-technologies. Low temperature operation of these devices can minimize thermally induced performance degradation mechanisms that lead to, for example, retention loss, limited endurance, broad distribution of programmed states, and so on. However, one challenge for the memory technologies working at cryogenic temperature is strong temperature dependence of switching voltage that can affect the energy requirements and write or access speed of the system.

Extensive studies on doped HfO_2-based ferroelectric thin films were done over last decade [1,8] toward their application in high-density, low-power, and high-speed electronics, and, most importantly, in NVM and non-volatile logic circuits. Among ferroelectric hafnia, Zr-doped HfO_2 (HZO) has received most attention thanks to its relatively low crystallization temperature, making it an excellent candidate for CMOS BEOL integration. [11, 12] However, wide industrial adaptation and commercialization of Hafnia-based FeRAM and FeFET based NVMs have not been realized yet, due to several important challenges such as, for example, low yield and performance uniformity over wafer scale, reproducibility of intermediate programmed states, and long retention and write endurance of the

FeFETs. To improve these performances, proper understanding of the ferroelectric film and interface properties, control over creation and dynamics of defect states under operating conditions are of major importance.

Cryogenic operation of FE memories has the potential to minimize ion movement within the FE layer and get more reliable operation until millions of programming and erasing cycles with identical values for the saturation and remnant polarization (P_S and P_r, respectively). Temperature dependent studies of ferroelectric materials also provide better insight of fundamental device physics that facilitates designing of engineered domain dynamics under different pulsing schemes, high retention and endurance. Traditional oxide perovskite devices based on $BaTiO_3$, $PbTiO_3$ or $Pb_{1-x}Zr_xTiO_3$ (PZT) studied extensively down to deep cryogenic temperatures [6, 13-15] provided many fundamental insights of the intricate material and interface physics. However, similar studies on the fluorite type binary oxide ferroelectrics, i.e., HfO_2 based ones, is rather limited, as the main driving force for HfO_2 based systems are their industry-scale memory performance that did not accommodate the difficulty and expense of cooling as most application domains require operation at ambience. It is known that that performance of conventional MOSFETs improve with lowering temperature due to an increase in channel mobility arising from decreased phonon scattering. Together with the hafnia based ferroelectric memories operating at 75 K and 4 K with desired properties, the demand for cryogenic memories can be met, reducing the huge energy consumption, thermal noise and delay of continuous data communication between quantum processors at deep cryogenic temperatures and memories operating at room temperature or power consuming and bulky electronics for heating up the space electronic components.

A few recent reports showed temperature-dependent studies on HZO capacitors with superconducting Niobium Nitride (NbN) electrode [16] and with commonly used Titanium nitride (TiN) electrode down to 4 K. [17, 18] Wang et al. [19] showed an improvement of memory window at cryogenic temperature for Si-doped HfO_2 FeFETs that comes with the obvious cost of increased programming and erasing voltages. To improve switching performance at cryogenic temperatures and design energy efficient cryo-memories, dynamic switching properties of the ferroelectric domains at cryogenic temperatures under fast programming pulses need to be understood properly and the FE gate-stack designed accordingly. The recent reports by Hur et al, [20, 21] showed excellent endurance performance of the HZO based two-terminal devices at 4 K exceeding 10^{10} cycles with 3.5 V operation. However, operation of HZO thin film capacitors over multiple polarization states, based on applied pulse amplitude and frequency over a wide temperature range have not been studied and therefore their potential for in-memory-computing (IMC) architectures have not been evaluated before.

In this work, we report temperature dependent polarization switching behavior of HZO thin film capacitors under wide range of pulse amplitudes and frequencies and evaluate the potential of these devices as analog memories operating down to 4 K. Our results show within the pulse voltage range of ±5V, large polarization switching can be obtained in HZO from 300 K to 4 K range with significantly improved endurance and analog properties at low temperature due to reduced movement of charged defects. The P_r value of 30 µC/cm^2 at 5 MV cm^{-1} field at 300 K reaches up to 75 µC cm^{-2} at 7 MV cm^{-1} field at 4 K with increased switching voltage, leading to memory window of 6 to 8 V depending on the operating frequency. High linearity and symmetry of analog states obtained below 100 K ensures possibility of reproducible 20 programming states that can lead to high-precision IMC operation near 77 K with these elements that can lower the cost of cooling and energy requirement for computing.

2. Results and discussion

2.1. Structural Characterization

In **Figure 1**, we present the structural characterization of two HZO reference thin films and of a metal-FE-insulator-metal (MFIM) device stack. The choice of MFIM stack was motivated by reports of Liu et al. [25] showing an ultrathin Al$_2$O$_3$ capping layer can improve ferroelectricity in HZO. The two HZO reference films were deposited on Si with native oxide and on TiN. In hafnia based ferroelectric devices, electrode materials sandwiching the ferroelectric film play a critical role in stabilizing the ferroelectric orthorhombic phase (*o*-phase). [26, 27] TiN is the most widely used electrode due to its low thermal expansion coefficient ($\alpha_{TiN} = 9.4 \times 10^{-6} \, °C^{-1}$) exerting the critical in-plane tensile stress to the HZO film to transform the HZO film to its *o*-phase during the rapid thermal annealing step. It was shown by Goh et al. [27] that by proper in-plane stress engineering, it's possible to maximize the *o*-phase and improve ferroelectric polarization in ultrathin HZO films, although the crystallization temperature needed for higher *o*-phase ratio often exceeded 600 ^{0}C. In our experiments, we kept the crystallization temperature fixed at 500 ^{0}C to keep the process suitable for CMOS back-end integration. We used PEALD grown TiN of 30 nm thicknesses that exerts an in-plane tensile stress of 100 MPa on the HZO grown on top of it. Here, it is important to mention that although it is generally believed that temperatures in the back-end processes should not exceed 450 °C, results in ref. 28 and 29 shows that the maximum annealing temperature depends on the structure and composition of the interconnection layers of the FEOL devices and high temperature annealing for prolonged time tends to increase in the interconnect resistance. However, the transistor characteristics, the silicide quality, and the leakage currents can remain unaffected even by annealing 90 min at temperatures up to 525 °C. [29]
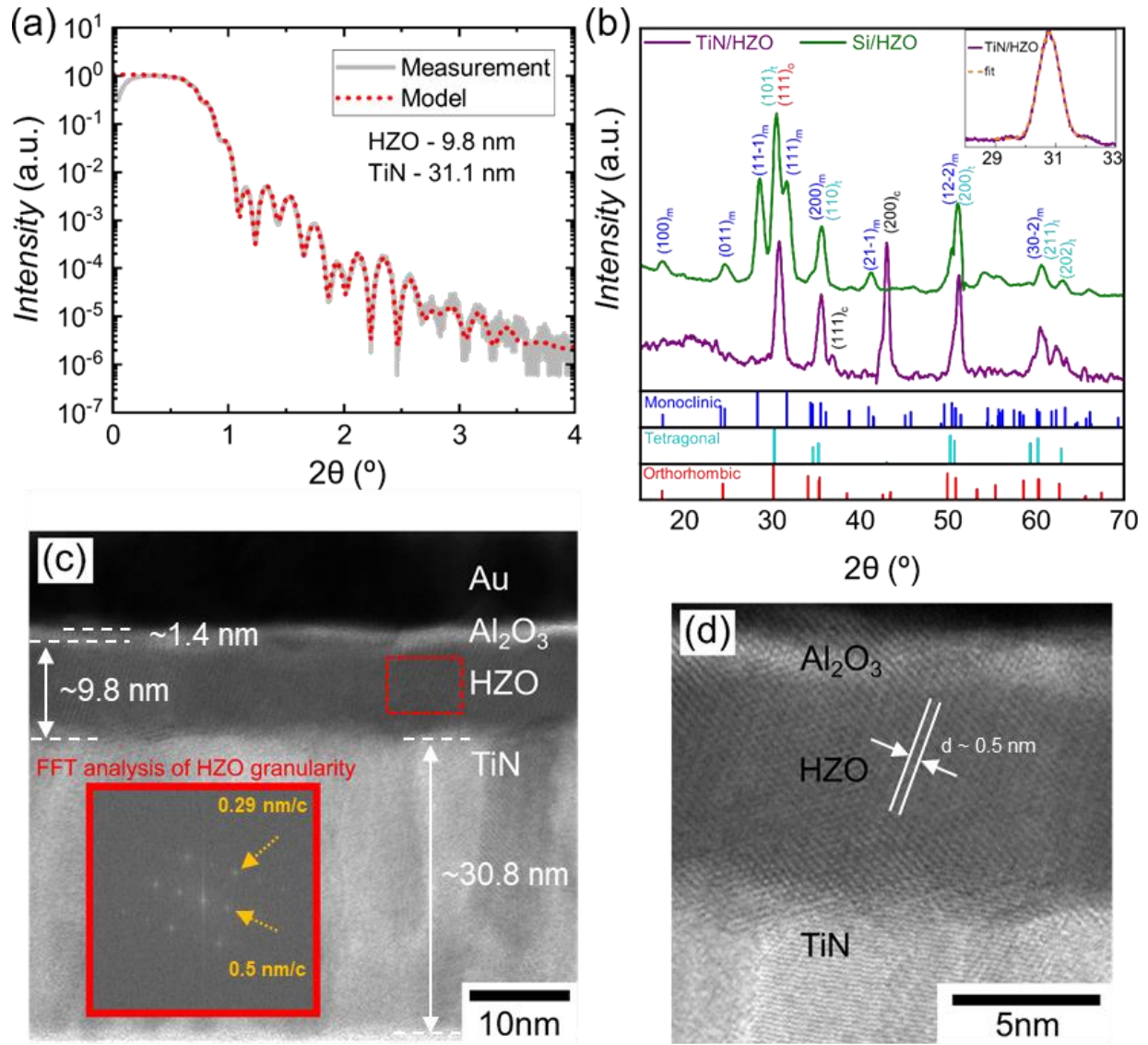
Figure 1. Structural characterization of HZO reference multilayers and MFIM stacks: (**a**) X-ray reflectivity oscillations of a TiN/HZO reference stack, with the fitting yielding 31.1 nm-thick TiN and 9.8 nm-thick HZO. (**b**) Out-of-plane GIXRD of HZO thin films grown on Si and TiN, capped with Al_2O_3. Powder diffraction intensities plotted in log-scale for monoclinic, tetragonal, and orthorhombic phases from references [22, 23, 24]. TiN Bragg peaks identified with *c*-phase subscript. Inset: Narrow-range scan over the predicted $(111)_o$ and $(011)_t$ peak positions for the TiN/HZO reference stack, with gaussian fit. (**c,d**) STEM imaging of the cross-section of the MFM device stack. Inset: fast Fourier transform of the HZO film with radial coordinates in nm/cycle for the two highlighted spots.

In **Figure 1(a)**, the X-ray reflectivity oscillations of the TiN/HZO reference stack ($Si/SiO_2/TiN/HZO/Al_2O_3$) were well modelled for 9.8-nm-thick HZO and 31.1-nm-thick TiN, in-line with the nominal deposition parameters. In **Figure 1(b)** we show the out-of-plane GIXRD diffractograms of the two HZO reference films collected for a wide-range 2θ scan between 10º and 110º (data smoothed with 5 points moving average), and a narrow-range high-resolution scan between 28º and 33º. The two diffractograms compare the growth of HZO on Si and TiN. The growth of HZO

on Si matches well to the results reported in [30] with the Bragg peak positions suggesting the coexistence of both monoclinic (*m*-phase, space group P2$_1$/c) and tetragonal phases (*t*-phase, space group P4$_2$/nmc). The diffractogram for the growth of HZO on TiN can be interpreted in the following ways: on one hand, assuming a polycrystalline growth as seen on Si, the absence of the orthorhombic (*o*-phase, space group Pca2$_1$ [30-34]) (010)$_o$ and (110)$_o$ Bragg peaks would suggest the stabilization of the *t*-phase; on the other hand, the preferential growth of TiN along (200)$_c$ (cubic, space group Fm$\bar{3}$m) can influence the growth of the HZO *o*-phase, complicating a clear distinction between *t*- and *o*-phases. In both films, the Bragg peaks are shifted towards higher angles (indicating out-of-plane compressive stress), compatible with the observed in-plane tensile stress determined from the wafer curvature. **Supplementary Table S1** summarizes the lattice parameters determined for the possible crystallographic phases on the two HZO reference stacks. The determination of the presence of the *o*-phase via an analysis of the overlapping (111)$_o$ and (011)$_t$ Bragg reflections, similar to reference [35], carries uncertainty due to the symmetric line shape shown on the narrow-range scan between 28º and 33º (see inset of **Figure 1 b**). Lower content of *o*-phase is generally expected from the 500 ºC RTA films [36] However, comparing both growths, the HZO films deposited on PEALD-grown TiN electrode had less pronounced monoclinic phase ratio in comparison to the HZO film grown and annealed under similar condition on Si substrate, indicating PEALD grown TiN to be a better substrate to promote ferroelectricity in low thermal budget HZO devices. The STEM imaging of the cross-section of the MFIM device confirms the nominal thicknesses of the deposited layers and the polycrystalline character of the TiN and HZO films (**Figure 1(c)**). A close inspection over the HZO layer shows clear lattice patterns spanning the entire thickness of the film, with the FFT analysis of the grains yielding a regular array of bright spots, highlighting the local crystalline character of the film (inset of **Figure 1(c)** and **1(d)**).

2.2. Electrical Characterization

Figure 2(a) shows the device schematics together with the electrical contacts for measurements. The ferroelectric transient current – voltage (*I-V*) and the corresponding polarization – voltage (*P-V*) hysteresis curves of the ferroelectric MFIM capacitors (TiN/HZO/Al$_2$O$_3$/Au) are shown in **Figure 2** and **3**, respectively at 8 different temperatures in 4 – 300 K temperature range. In our experiments, we initially characterized the HZO capacitors both in pristine state without any wake-up cycle protocol and with a pre-pulsing protocol of 5×10^3 positive-up-negative-down (PUND) pulses at $V_{PUND} = 9$ V$_{pp}$ at $f_{PUND} = 500$ Hz prior to measurements. Although devices without any pre-pulsing already show open hysteresis with similar P_r value and switching field as the pulsed sample (shown in **Supplementary Figure S1**), showing wake-up free operation of these devices is also possible.

However, higher reproducibility of properties under the pre-pulsing scheme prompted us to follow this protocol throughout all the measurements under wide temperature range.
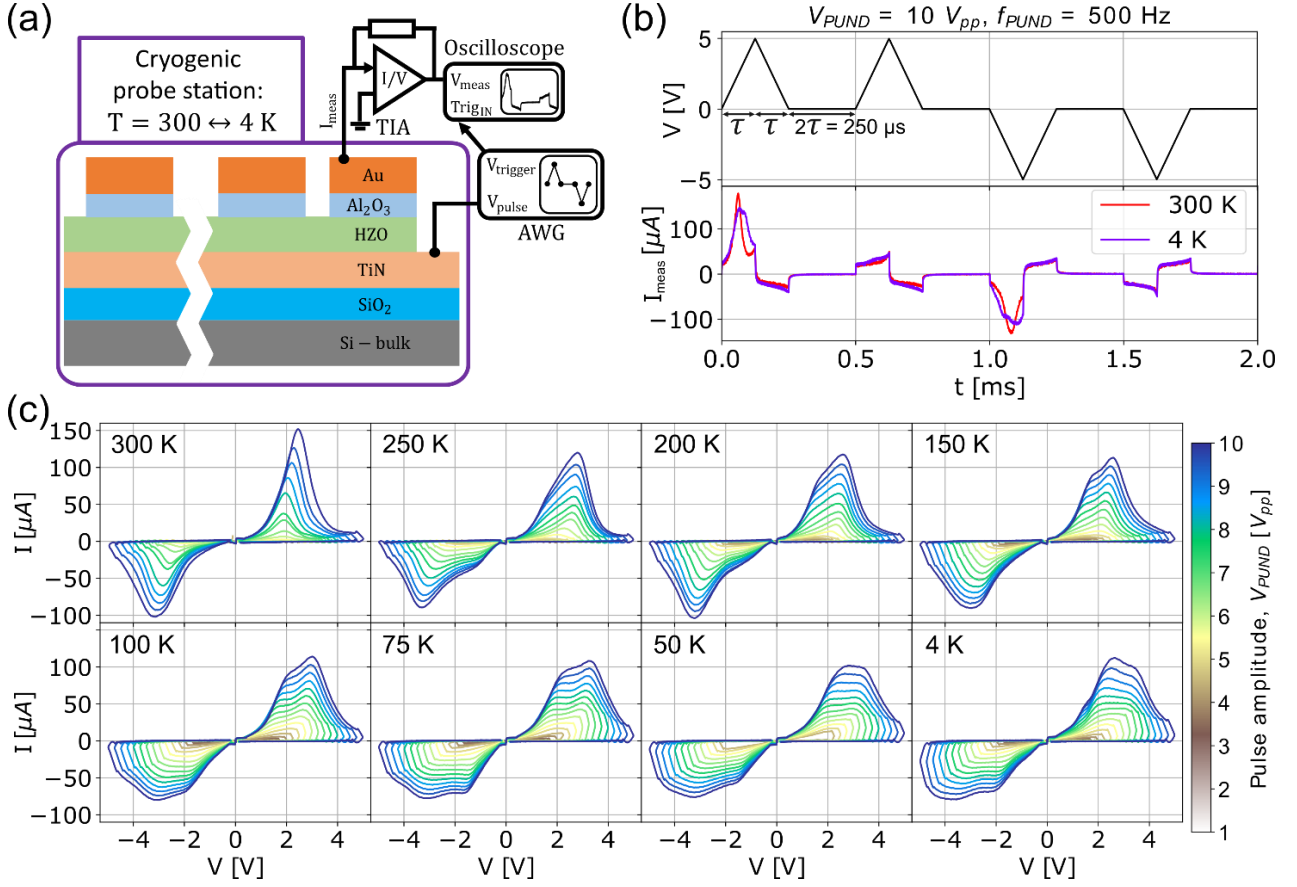

Figure 2. Measurement setup and transient current-voltage characterization using the PUND pulse sequence with frequency 500 Hz from 300 K down to 4K: (a) Device cross-sectional schematic with electrical characterization setup featuring cryogenic probe station, transimpedance amplifier (TIA), arbitrary waveform generator (AWG), and oscilloscope. (b) Positive-up negative-down (PUND) waveform used to characterize the HZO ferroelectric properties. An example of voltage-time dependence for the pulse amplitude $V_{PUND} = 10$ V$_{pp}$ (peak-to-peak voltage) at PUND cycle frequency (f_{PUND}) = 500 Hz is shown in top panel. f_{PUND} = 500 Hz corresponds to pulse rise and fall times $\tau = 125$ µs and the delay of $2\tau = 250$ µs. The bottom panel shows examples of the measured current (I_{meas})-time t) response at 300 K and 4 K. **(c)** Transient current-voltage (*I-V*) characteristics obtained from PUND with non-ferroelectric related current component subtracted. f_{PUND} = 500 Hz and V_{PUND} = from 0.5 to 10 V$_{pp}$ (with the step of 0.5 V$_{pp}$) were used to characterize the individual devices between 300 K and 4 K. All devices were measured from the same die. To avoid any possible fatigue effects (among others), for each temperature point, an individual device was measured. *I-V* characteristics with different V_{PUND} were measured from the same device.

The $I - V$ measurements were obtained using a PUND voltage scheme, which is one of the most used techniques to accurately measure the saturation (P_S) and remnant polarization (P_r) values of FE capacitors. We used triangular pulses of 500 Hz frequency and a voltage amplitude of up to ±5 V.

The PUND pulse sequence (V-t) and the corresponding current traces (I_{meas}-t) at 300 K and 4 K are shown in **Figure 2 (b)** top and bottom panel, respectively. The total measured current (I_{meas}) of the first pulse includes polarization current (I), leakage current (I_{Lk}), and dielectric current (I_{DE}). Due to application of the positive voltage pulse, the polarization, **P**, points to the bottom TiN substrate (P↓) while for negative applied pulse, the **P** points towards the top Au electrode (P↑). The current response of the device due to the first pulse (the switching pulse with current I_{switch}) consists of all current components while that due to the second pulse (the non-switching pulse with current $I_{non-switch}$) consists of only the non-FE components. The FE polarization current can, therefore, be obtained by $I = I_{switch} - I_{non-switch}$. Current I is free from non-FE current components (device leakage and dielectric current and experimental setup effects) that enables correct estimation of the polarization value and is followed in this work. From **Figure 2(c)** we see that, upon cooling the samples from 300 K to 250 K the transient current magnitudes drops slightly, however, not dropping further from 250 K to 4 K. Below 200 K, a peak broadening feature starts to appear in the transient $I - V$ characteristics which becomes more prominent below 150 K indicating more gradual nature of polarization switching and absence of full polarization rotation within the applied ±5V range. This peak broadening feature becomes even more prominent below 50 K with the I remain nearly same within ±5V range. Gradual switching at low temperature can be explained by impeded FE domain wall motion due to lack of enough thermal energy. Application of higher magnitude pulses can produce very high P_r values at low temperatures (see below).

The high FE polarization current in HZO capacitors resulted in a high polarization value calculated using the equation $P = \frac{1}{A} \int_{t_2}^{t_1} I \, dt$, where A denotes the area of the capacitor and $t_1 - t_2$ being the time window of the applied pulse. $2P_r$ value of $\sim$ 60 μC cm^{-2} at room temperature (**Figure 3**) is observed for the capacitors, which is among the state-of-the-art values for HZO capacitors annealed at 500 °C and is the highest where no capping electrodes or wake-up protocols were used during the HZO crystallization. Here $2P_r$ is calculated as 2* |+P_r| due to nearly identical values of |+P_r| and |-P_r|. Our results are benchmarked against the state-of-the-art values in **Table 1**. High $2P_r$ value is generally attributed to an enhanced formation of polar o-phase leading to a greater ferroelectric polarization. [30] In our HZO, we believe this is resulted from large in-plane tensile stress exerted by the PEALD grown TiN on the HZO film, as can be seen from **Figure 1(b)**, when compared with HZO film grown on Si. The samples were annealed without any top electrodes (as discussed in Methods section) and high $2P_r$ value in films, even without standard wake-up protocol, confirms that there is no need for a special capping metal layer for obtaining a high P_r in our devices. This ensures free choice of top electrode in the device stack, increasing design flexibility.

With decreasing temperature, the P_r decreased initially (for ±5 V pulsing cycles) showing nearly a minimum around 250 K that eventually increases due to further cooldown until 100 K (see **Fig. 3**). Below 100 K, the P_r value does not change much. Additionally, below 150 K, a peak broadening in the transient *I-V* curves (as shown in **Figure 2**) leads to a little distorted *P-V* loops (**Figure 3**). This feature can mainly be attributed to the incomplete polarization switching at low temperature due to lack of enough electrical and thermal energy to fully switch all domains.

For an ideal ferroelectric with rectangular *P-V* hysteresis loop (neglecting the linear dielectric response), the application of a voltage $V \geq Vc$, the coercive voltage, will induce a complete polarization switching and no reorientation of spontaneous polarization is expected for $V < Vc$. However, for practical devices, *P-V* hysteresis loops are more gradual, and the corresponding switching current peaks are broadened indicating a distribution of switching fields due to different domains switching at slightly different fields. Therefore, to obtain a fully saturated *P-V* hysteresis loop, an applied voltage (V_S) of 2–3Vc is needed. Under a lower applied voltage, only a fraction of the domains switch polarization resulting in a minor-loop hysteresis. In the present experiments, appearance of peak broadening below 150 K indicates some pinned domains require higher switching voltages and the applied field strength is not enough to reach saturation for them. This indicates at low temperature, application of higher amplitude pulses could improve Ps and P_r values. The values of V_c and V_S depend on the material properties including the distribution of grain size, amount of non-polar phase portions at the interface or in the bulk. For a fixed sample, these parameters also strongly depend on the measurement conditions like temperature and frequency of applied voltage pulse.

When the devices are operated between multiple peak-to-peak voltage (V_{pp}) ranges, devices showed polarization minor-loop hysteresis **(Fig. 3)**, representative of multiple intermediate polarization states with smaller P_r, Vc and memory window (MW) with decreasing V_{pp}. With decreasing voltage amplitude, the recorded minor hysteresis loops showed more pronounced shift in negative coercive voltage, V_{c-} compared to positive coercive voltage V_{c+}, more prominently down to 150 K indicating easier domain rotation in one direction compared to the other.

Asymmetric switching field and higher voltage requirement for switching from P↑ to P↓ indicate presence of significant internal bias fields in our devices. The internal bias field can arise in a FE thin film due to dissimilar electrode configuration on the two sides of the FE and accumulation of pre-existing charged defects that creates pinning centers prohibiting the FE-domains from switching. A sufficiently high electric field can overcome the pinning potential making the FE-domains de-pinned from the charged defects and make their rotation possible. This leads to an effective increase in the switching voltage. From Figure 3, we see that V_{C-} is higher than V_{C+} and has less temperature dependence. This observation points to the fact that charged defect related pinning of FE domain

plays the major role in our devices for P↑ to P↓ rotation compared to lack of thermal energy related increase in switching voltage. In HZO, most charged defects are positively charged oxygen vacancies, either pre-existing in the film during fabrication or generated during electric field cycling. Inhibited switching from P↑ to P↓ indicate the bottom electrode interface (TiN/HZO) acts as reservoir of oxygen vacancy related defects where positively charged vacancies prohibit the rotation of positive polarization bound charges. Considering the tendency of TiN to scavenge oxygen from HZO, this inference is plausible, however, a thorough understanding of interface defects through *in-operando* structural characterization would be needed for further clarification. In comparison to V_{C-}, the temperature dependence of V_{C+} show trend similar to traditional FE devices, [13] indicating that the FE domain switching, assisted by thermal energy is the dominating mechanism. Increase in P_r below 200 K in our devices, instead of slight decrease in magnitude of I might have its origin.
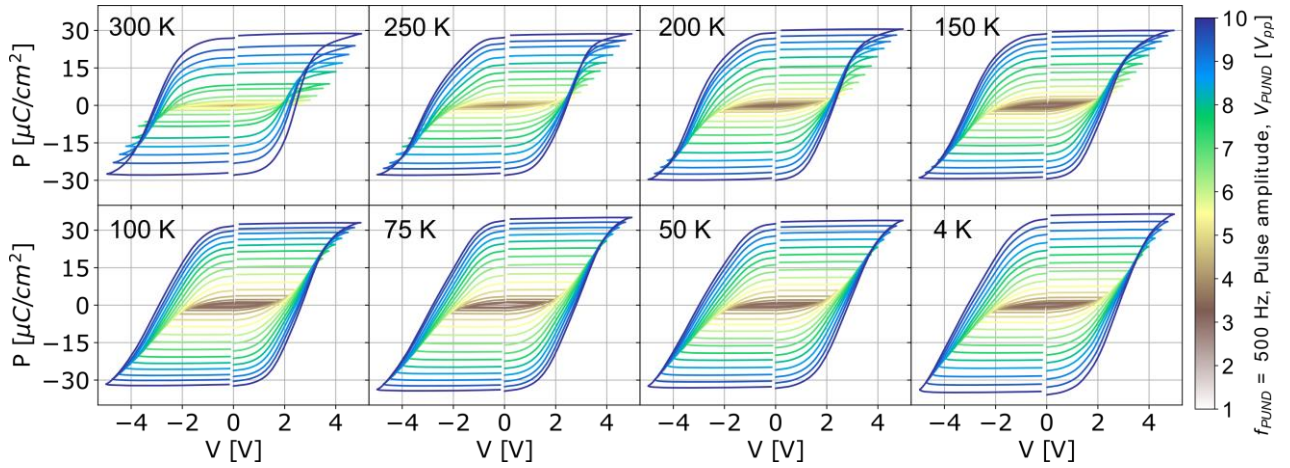

Figure 3. Polarization-voltage characteristics for different PUND pulse amplitudes from 300 K down to 4 K at PUND frequency of 500 Hz: To obtain these *P-V* characteristics, the *I-V* data from **Figure 2 (c)** measured with V_{PUND} = from 0.5 to 10 V_{pp} (with the step of 0.5 V_{pp}) were integrated and normalized by the device area of $100 \times 100 \, \mu m^2$. All devices were measured from the same die.

2.2.1. Statistical variation of key performance indices

To quantify polarization switching distribution of the fabricated devices, we measured large number of devices from multiple dies, both at 300 K and 4 K and extracted their P_r, V_{c+}, V_{c-} and MW distribution, as shown in **Figure 4**. At 300 K, measured 87 devices showed distribution of $2P_r$ values ranging from $25 - 60 \, \mu C \, cm^{-2}$ with some devices showing even up to values of $80 \, \mu C \, cm^{-2}$. However, most devices had values concentrated near $45 \, \mu C \, cm^{-2}$. The distribution of V_{c+} values showed range between 2.35 to 2.7 V with a maximum around 2.4 V while that for V_{c-} range from -2.9 to -3.6 V with maxima around -3V showing a wider variation of switching voltage values while switching polarization direction from P↓ to P↑. The MW, calculated as $(V_{c+} - V_{c-})$ consequently showed a

distribution of values between 5.2 to 6.2 V with a peak around 5.4 V. At 4 K, within 54 measured devices, a significant distribution was still observed, however, the P_r maxima were nearly at the same value compared to 300 K. The V_{c+} ranges between 2.75 to 3.45 V with peak at around 3 V while V_{c-} ranges between -3.45 to -3 V with peak at around -3.2 V. These two peak values indicate more symmetric switching at 4 K compared to 300 K with increase of MW by almost 0.6 V due to lowered temperature. The distribution in switching parameters were measured also at different other temperatures and two other frequencies of 5 kHz and 25 kHz (shown in Fig. S2 and S3) that shows the switching distribution is more or less independent of temperature and measurement frequency.
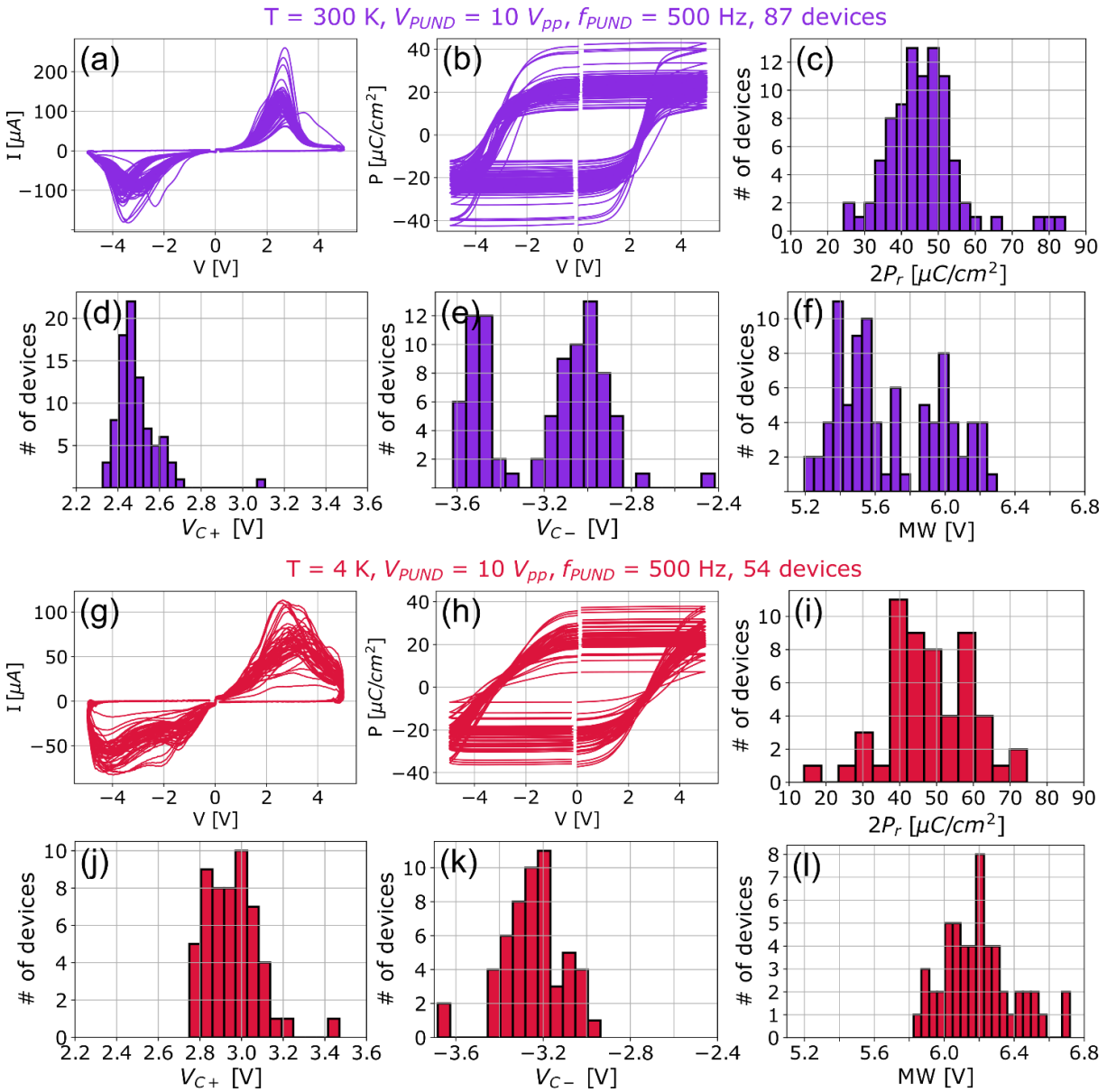

Figure 4. Variability of key ferroelectric device parameters from a 150 mm wafer: remnant polarization, coercive voltages and memory window at 300 K and 4 K. In **(a,g)** I-V and **(b,h)** P-V characteristics of measured 87 (54) individual devices from 4 (7) individual dies, labeled as without relation to their positioning on the wafer as {"A", "E",

"H", "L"} and {"A", "D", "E", "M", "N", "L", "K"} respectively, are shown for T = 300 K (4 K). The histogram distributions of polarization ($2P_r$), positive (V_{C+}) and negative (V_{C-}) coercive voltages, and memory window (MW) are shown in **(c,i)**, **(d,j)**, **(e,k)**, and **(f,l)** for 300 K and 4 K respectively.

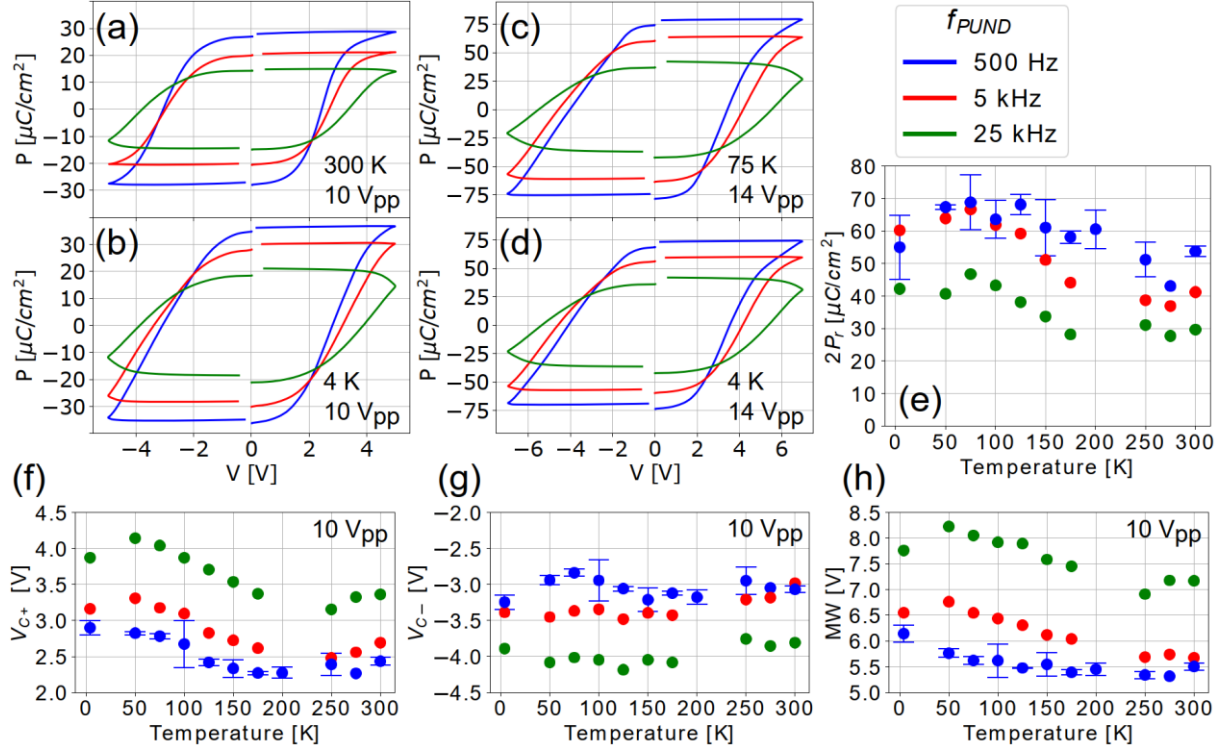## *2.2.2. Frequency dependence of polarization switching*

Figure 5. Frequency and temperature dependences of Polarization, Coercive Voltages and Memory Window at fixed pulse amplitude from 300 K down to 4 K: (a,b) *P-V* characteristics of HZO devices at fixed V_{PUND} = 10 V_{pp} and different f_{PUND} of 500 Hz, 5 kHz and 25 kHz at 300 K and 4 K. **(c,d)** *P-V* characteristics with the critical pulse amplitudes (close to breakdown) V_{PUND} = 14 V_{pp} at different f_{PUND} at 75 K and 4 K. $2Pr$ as high as 150 $\mu C cm^{-2}$ was measured at 4 K and 75 K. **(e)** $2Pr$ as a function of temperature T at fixed V_{PUND} = 10 V_{pp} and different f_{PUND} (the rise/fall time constants corresponding to each f_{PUND} are given in the legend). The coercive voltage dependences are given in **(f)** V_{C+} and **(g)** V_{C-}, plotted as a function of T at different f_{PUND} and V_{PUND} = 10 V_{pp}. **(h)** Temperature dependence of MW at different f_{PUND}. All devices were measured from the same die coming from a 150 mm wafer. To avoid the fatigue effects (among others), for each temperature point, an individual device was measured. Moreover, *P-V* dependencies with different f_{PUND} and V_{PUND} = 10 V_{pp} (or 14 V_{pp}) were measured from the same device. Due to non-negligible device-to-device variation, error bars are added to the data measured between (e-h) for representative curves plotted at f_{PUND} of 500 Hz. The measurements on which the error bar is calculated are shown in Figure S2.

An experimental investigation on frequency-dependent polarization switching at different temperatures are presented in **Figure 5**. *P-V* hysteresis loops of HZO capacitors at three different frequencies at 300 K and 4 K are shown in **Figure 5(a)** and **(b)** respectively, for pulse amplitude of 10 V_{pp}. The switching dynamics and coercive fields of ferroelectrics generally shows a significant

frequency dependence, [37, 38] that is, when the amplitude of the cycling field is fixed, the change in its frequency results in a different polarization reversal state for the FE film. And therefore, the number of domains involved in the switching will also change significantly. Increasing frequency resulted in lower P_r and increased V_c values. In our HZO samples V_c values does not change significantly when the frequency is increased from 500 Hz to 5 kHz. However, from 5 to 25 kHz, both V_{c+} and V_{c-} values increases significantly and the same trend is seen both at 300 K and 4 K. **Figure 5(c)** and **(d)** shows P-V curves up to 14 V_{pp} taken at 75 K and 4 K respectively at 500 Hz, 5 kHz and 25 kHz. This result shows that HZO devices can withstand large amplitude voltage pulses at low temperatures due to reduced ion movements that leads to early breakdown at higher temperatures. Also, application of 14 V_{pp} pulse led to record high P_r value of 75 µC cm^{-2} from HZO capacitors reported till date. **Figure 5(e-h)** shows temperature dependence of P_r, V_{c+} and V_{c-} and MW values at three different frequencies for applied pulsed voltage of 10 V_{pp}. As mentioned previously for 500 Hz, P_r shows a dip around 250 K followed by an increase below 200 K. For 5 kHz and 25 kHz frequencies a similar trend in temperature dependence is observed. The temperature dependence of coercive voltages and MW (**Fig. 5 f-h**) shows negligible temperature dependence of V_{c-}, however V_{c+} increasing with decreasing temperature, and therefore increasing the MW significantly below 50 K for all different frequencies. At cryogenic temperatures, increase in P value under similar electric field seems counter intuitive since increase in V_c would result in lesser number of ferroelectric domains to switch. Therefore, slight increase in P_r at low temperature might be due to suppression of electronic leakage contribution that neutralize the positively charged oxygen vacancies and reduce the polarization at high temperatures. However, significant device-to-device variation poses some ambiguity on the conclusion whether the observed increase in P_r at low temperature is a real effect. More experiments will be needed to confirm the hypothesis. In Figure 5 (e-h), error bars are added indicating the standard deviation around the mean value in the temperature dependence of P_r, V_c and MW for a certain PUND frequency of 500 Hz. The measured data and number of samples used to extract P_r, V_c and MW for each temperature point are given in Supplementary Information, Fig. S2.

2.2.3. Amplitude dependence of polarization switching

Figure 6 (a-d) shows the pulse amplitude dependence of polarization hysteresis at 4 K and 75 K with frequency of 500 Hz. In our devices the maximum V_{pp} that we could successfully apply, without suffering an early breakdown, is 10 V at room temperature and at 250 K. Above 10 V, the devices broke down after a few cycles. However, at temperatures below 200 K, devices were able to withstand much higher amplitude voltage pulses reaching up to 14 V below 75 K and leading to very high $2P_r$ values. Highest $2P_r$ value of 150 µC cm^{-2} is obtained at 75 K with applied pulse of magnitude 14 V_{pp}

that remains nearly same down to 4 K. Temperature dependence of P_r, coercive voltages and MW for different pulse amplitudes are shown in **Figure 6 (e-h)**. The curves presented in Figure (e-h) also represent the maximum pulse amplitude that the devices could handle over multiple switching cycles at each measured temperature, indicating maximum switchable polarization at each temperature. The increased breakdown voltage at low temperature in our HZO devices can be explained by the fact that at higher temperatures, thermally activated inelastic tunneling through defect states in the HZO layer causes charged oxygen vacancies to move more easily under the combined effects of electric fields and temperature, causing non-negligible leakage currents. This positive ionic charges over a longer period of time causes bias-induced stress inside the device, leading to device fatigue and eventual oxide breakdown, similar to time-dependent-dielectric breakdown (TBBD) as previously reported in HZO FeFETs ref. [39]. At lower temperatures, due to limited diffusion of oxygen vacancies, the leakage current contribution decreases significantly, increasing the breakdown field and improving the device lifetime.
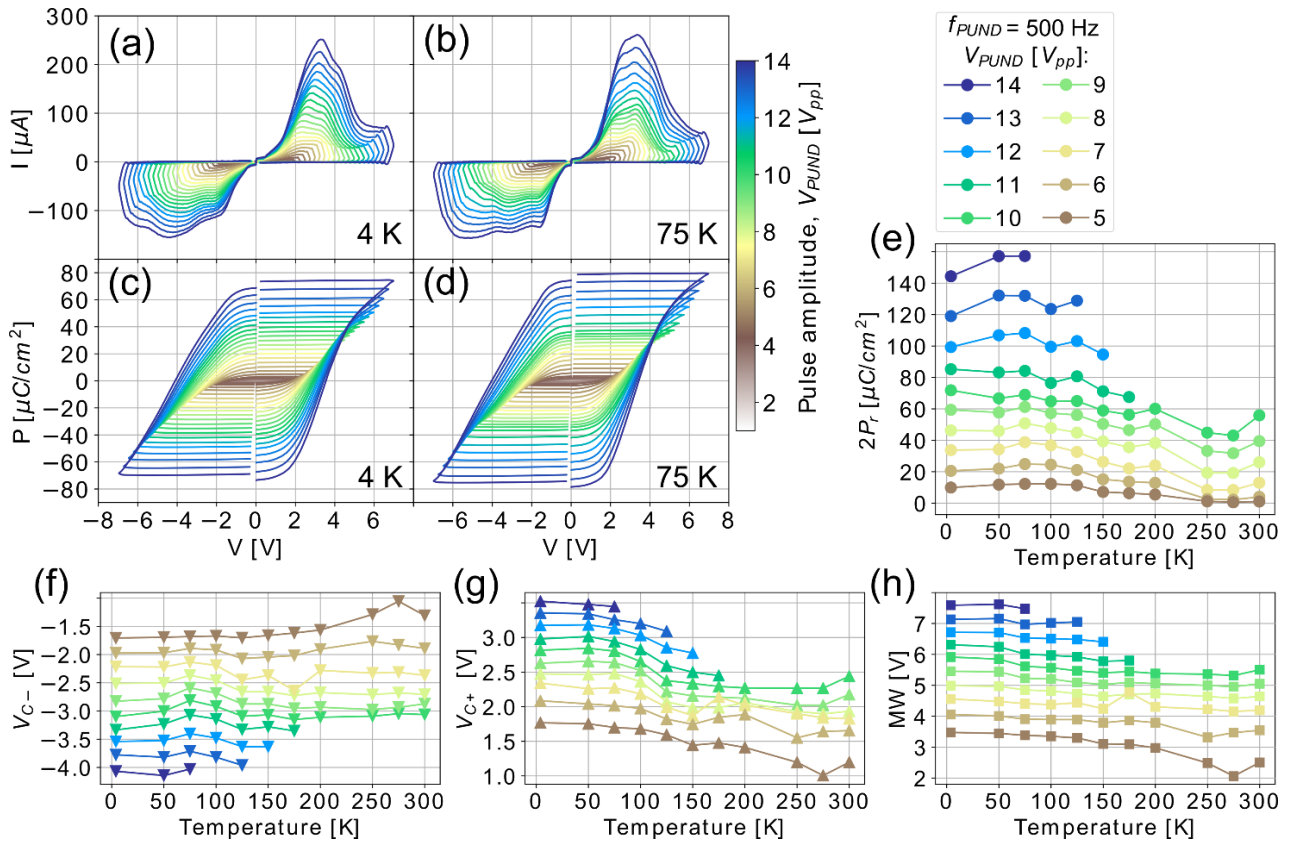

Figure 6. Pulse amplitude and temperature dependences of Polarization, Coercive Voltages and Memory Window at fixed frequency from 300 K down to 4 K: Transient $I-V$ **(a,b)** and corresponding P-V characteristics **(c,d)** for V_{PUND} from 2 to 14 V_{pp} with a step of 0.5 V_{pp} at 4 K measured at f_{PUND} = 500 Hz are shown for T = 4 K and 75 K respectively. Almost linear increase of polarization with pulse amplitude can be observed (see Figure 8 for more detailed analysis). The temperature dependence of polarization is shown in **(e)**. As the temperature was reduced, the critical breakdown pulse

amplitude was gradually increased from 10 V_{pp} at 300 K to 14 V_{pp} at T ≤ 75 K. The coercive voltage dependences are given in **(f)** V_{C-} and **(g)** $V_{C+,}$ plotted as a function of T for different V_{PUND} and f_{PUND} = 500 Hz. **(h)** Temperature dependence of MW at different V_{PUND}. All devices were measured from the same die coming from a 150 mm wafer. For each temperature point, the same individual devices as analyzed in Figure 5 were also studied for the amplitude dependence.
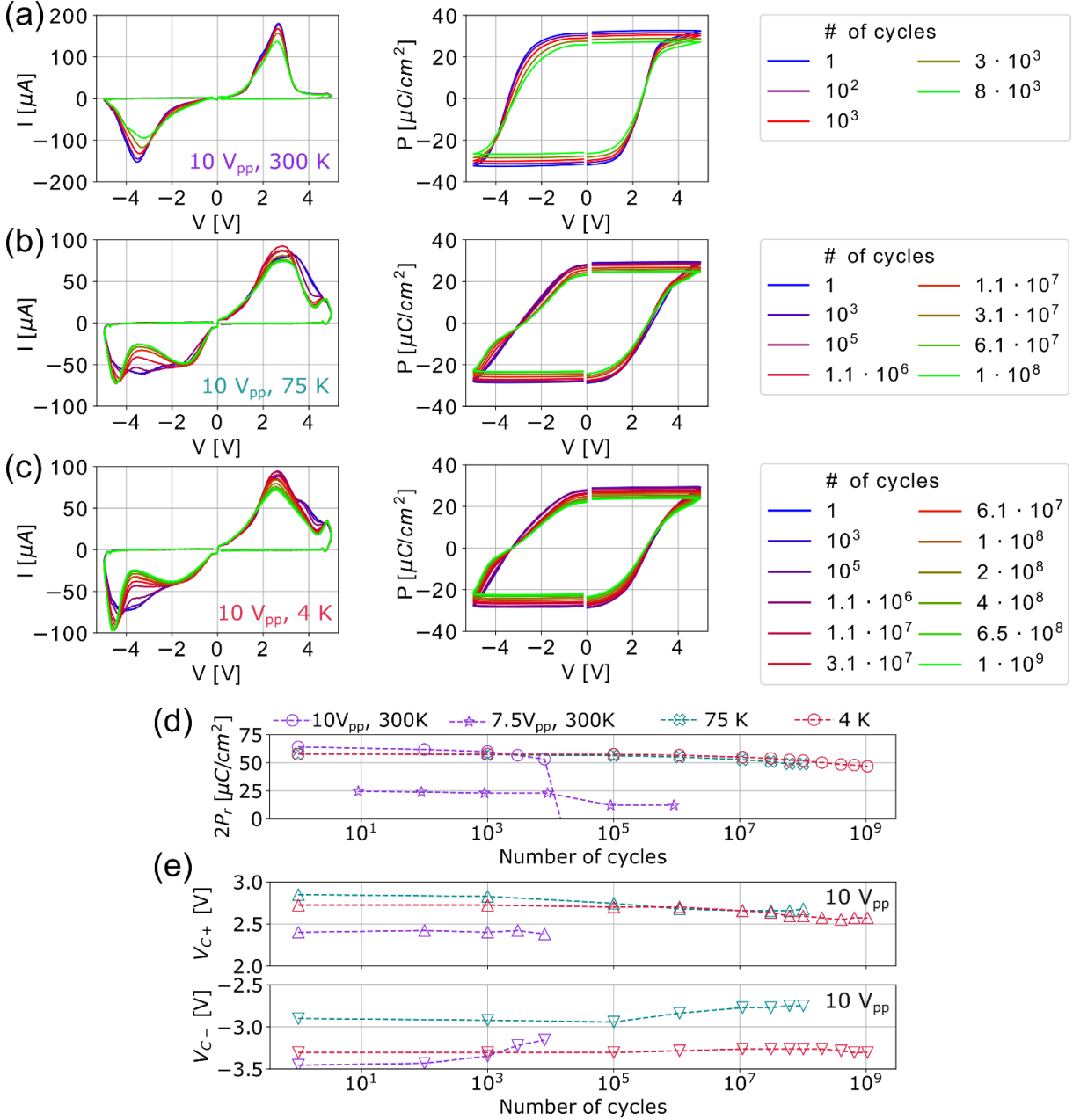
2.2.4 Imprint, fatigue and endurance

Figure 7. Fatigue and endurance effects at 300 K, 75 K, and 4 K. *I-V* and *P-V* curves measured at different pulse cycles are shown in **(a)**, **(b)**, and **(c)** for T = 300 K, 75 K, and 4 K, respectively. Standard periodical sawtooth pulses at f_{stress} = 100 kHz and stress pulse amplitude V_{stress} identical to read amplitude $V_{PUND-read}$ = 10 V_{pp} amplitude were used for cycling, and after each step from 1 cycle to 8×10³, 10⁸, 10⁹ at 300 K, 75 K, and 4 K respectively, the PUND measurements were done at $f_{PUND-read}$ = 500 Hz. While at 300 K using 10 V_{pp}, the device breaks down before 10⁴ cycles, at 75 K and 4 K, the devices survive more than 10⁸ and 10⁹ number of cycles, respectively. While the *I-V* waveform deformation at

after a large number of cycling steps can clearly be observed in **(b)** and **(c)**, the corresponding *P-V* characteristics show that no critical fatigue occurs. **(d)** The polarization as a function of cycling steps with 10 V_{pp} at 100 kHz and $f_{PUND-read}$ = 500 Hz is showed for 300 K, 75 K, and 4 K with the circle markers. Additionally, 300 K data for 7.5 V_{pp} measured using the same frequency. (e) The evolution of V_{c+} (top) and V_{c-} (bottom) as function of switching cycles are shown for different temperatures. 300 K data at 10 V_{pp} were measured from one die, 300 K data at 7.5 V_{pp} were measured from another die, and 4 K and 75 K were obtained yet from another die.

Next, we view the effect of field cycling on P_r, V_{C+} and V_{C-}. Imprint effect and temperature dependence of imprint effect in our devices was discussed above in the light of charge injection causing one polarization state to stabilize at the expense of the opposite polarization state. [40, 41] In **Figure 7**, the evolution of imprint, fatigue and endurance properties of our HZO capacitors are shown at three different temperatures of 300 K, 75 K and 4 K. At room temperature (**Figure 7 (a)**), the *P – V* hysteresis loop show significant degradation and hard breakdown due to ~10 000 field cycling when operated within 10 V_{pp} range at 100 kHz frequency. With 7.5 V_{pp}, however, the devices sustained more than 10^6 pulse cycling. A slight fatigue was observed with small reduction in P_r after 10^4 cycles, but no significant change in V_{c+} was observed. V_{c-}, however showed a degradation after 10^4 cycles. At 75 K and 4 K (**Figure 7** (**b** and **c**), respectively), devices showed much improved endurance performance upon 10 V_{pp} field cycling. Beyond 10^6 cycles, a little distortion in the *I-V* started to appear, resulting in appearance of double peak structures in the *I-V*s and a distorted *P-V* loop at 75 K and 4 K. This sub-cycling features in *I-V*, as also observed by Li et al., [42] arises from incomplete polarization rotation due to fatigue, and it is observed that up to 10^7 cycles, the fatigue is reversible to the major extent. However, after 10^8 cycles at 100 kHz, the device performance is permanently affected, and the initial $2P_r$ values could not be recovered. The sub-cycling behavior in [42] was explained by a progressive building up of local bias fields and pinning of domains. In our experiments, it is noteworthy to mention that more pronounced sub-cycling behavior is seen on the negative polarity side, (feature that has been discussed with respect to **Figure 3**).

This observed fatigue behavior based on temperature can be explained qualitatively by considering the interplay between ferroelectricity and ionic transport in the ultrathin HZO capacitor layers. In general, degradation of device switching properties are attributed to the interface trap states and charged defect generation at the HZO interface with the electrode upon repeated bipolar switching of the polarization during field cycling. Majority of the charged defects in the HZO film is positively charged oxygen vacancies. At low temperature, delayed or absence of degradation at both 75 K and 4 K (**Figure 7(b)** and (**c**)) can be attributed to the suppression of thermally assisted movement of the charged ions within the bulk FE film and at the FE - electrode interface. Furthermore, the observation that cycling dependence of P_r and V_{c+} are nearly identical whereas degradation in V_{c-} starts at earlier

cycles, leads to the conclusion that charged defect related effects are responsible for degradation of device performance and need to be understood and improved. For a quantitative explanation of degradation mechanism, a thorough characterization and modelling of defect state generation and evolution under bias stress is needed. In ALD grown polycrystalline oxide FEs, interplay of different effects is much more complex than what can be inferred from classical electrostatic models based on polarization charge effects and improvement of room temperature performance would need FE layer and interface optimization based on understanding of defect mechanism.

While discussing the fatigue and breakdown, leakage current values are essential to take into account and we have tabulated the values in SI, table S2, comparing our results with results from other articles. However, it is important to consider here that all the reported values are from large sized capacitors with 100x100 um^2 area, where the main conduction mechanism is trap-assisted tunneling. Presence of large numbers of grain boundaries and other structural defects in large sized capacitors makes the trap assisted tunneling more probable increasing the leakage currents. In devices smaller than 1 µm^2, which would be relevant for densely integrated memory circuits, the leakage current is expected to be significantly reduced, that would improve the performance and energy efficiency of the cryogenic memory circuits. Future experiments will focus on these improvements.

Table 1. Comparison between this work and several previously reported cryogenic HfO$_2$-based ferroelectric devices (refs. [16-18,20,21,43]) in terms of key performance matrices at room temperature and at low temperature.

Stack: from top electrode to bottom electrode	HZO growth method, annealing temp. and time	P$_r$ at room temp. and elec. field	P$_r$ at low temp. and elec. field	E$_C$ at the lowest measured temp.	Endurance at room temp. / cycling amplitude and freq.	Endurance at low temp. / cycling amplitude and freq.	Reference
_Au (50 nm)_ _Al₂O₃ (1.2 nm)_ _HZO (10 nm)_ _TiN (30 nm)_	ALD, 500 °C, 30 s	**300 K:** (a) **30 µC/cm^2** @ 4.4 MV/cm (b) **12 µC/cm^2** @ 3 MV/cm f_{PUND} = 500 Hz _(highest Pr at lowest freq. f_{PUND} = 500 Hz are given)_	**4K:** (a) **75 µC/cm^2** @ 6.2 MV/cm (b) **35 µC/cm^2** @ 4.4 MV/cm (c) **17 µC/cm^2** @ 3 MV/cm _(highest Pr at lowest freq. f_{PUND} = 500 Hz are given)_	**4K :** $E_{C+} \approx$ 3 MV/cm $E_{C-} \approx$ 3.2 MV/cm _(asymmetric dev.)_ _(f_{PUND} = 500 Hz)_	**300K:** (a) **>10^6 cycles** @ 3.75V$_p$ / 100 kHz _(fatigue)_ (b) up to 10^4 cycles @ 5V$_p$ / 100 kHz _(hard breakdown)_	**4K:** (a) **>10^9 cycles** @ 5V$_p$ / 100 kHz _(non-critical fatigue)_ (b) up to 10^8 cycles @ 6V$_p$ / 25 kHz _(hard breakdown)_ (b) up to 10^7 cycles @ 7V$_p$ / 25 kHz _(hard breakdown)_	This work*
_Al (100 nm)_ _TiN (12 nm)_ _HZO (10 nm)_ _TiN (12 nm)_	ALD, 450 °C, 30 s	**300 K:** 20 µC/cm^2 @ 3.5 MV/cm f_{PUND} = 83.3 kHz	**4 K:** (a) 18 µC/cm^2 @ 3.5 MV/cm (b) 10 µC/cm^2 @ 2.5 MV/cm f_{PUND} = 83.3 kHz	**4 K:** 2 MV/cm _(symmetric dev.)_	**300 K:** (a) 2 × 10^7 cycles @ 2.5 V$_p$ / 33.3 kHz _(hard breakdown)_ (b) 10^6 cycles @ 3.5 V$_p$ / 33.3 kHz _(hard breakdown)_	**4 K:** (a) 3.5 × 10^{10} cycles @ 2.5 V$_p$ / 33.3 kHz (b) 1.1 × 10^{10} cycles @ 3.5 V$_p$ / 33.3 kHz _(hard breakdown)_	[Hur et al. IEEE JXCDC 2021]

		300 K / 293 K	77 K / low T	E_C	Endurance 300 K	Endurance 77 K / low T	
_Al (100 nm)_ _TiN (12 nm)_ _Al₂O₃ (2 nm)_ **_HZO (10 nm)_** _TiN (12 nm)_	ALD, 450 °C, 30 s	**300 K:** ~ 17 µC/cm² @ 6 MV/cm f = 10 kHz	**77 K:** ~ 20 µC/cm² @ 6 MV/cm f = 10 kHz	**77K:** $E_{C+}≈4.4$ MV/cm $E_{C-}≈2.8$ MV/cm *(asymmetric dev.)*	**300 K:** 2 × 10³ cycles @ 6 V$_p$ / 10 kHz *(hard breakdown)*	**77 K:** > 10⁵ cycles @ 6 V$_p$ / 10 kHz breakdown happens at 10⁷	[Hur et al., IEEE TED 2022]
_Pt (xx nm)_ _TiN (xx nm)_ **_HZO (6.7 nm)_** _TiN (xx nm)_ _Pt (xx nm)_	ALD, 400 °C, x s	**300 K:** ~ 22 µC/cm² @ 2 MV/cm	**77 K:** ~ 27 µC/cm² @ 2 MV/cm **150 K:** ~ 26 µC/cm² @ 2 MV/cm	**77K:** ~ 1.8 MV/cm *(symmetric dev.)*	—	—	[Xing et al., IEEE JEDS 2022]
NbN (200 nm) **_HZO (20 nm)_** _NbN (150 nm)_	ALD, 600 °C, 30 s	**293 K:** ~ 5 µC/cm² @ 2 MV/cm	**4 K:** ~ 11 µC/cm² @ 2 MV/cm **150 K:** ~ 9 µC/cm² @ 2 MV/cm	**4K:** ~ 1 MV/cm *(symmetric dev.)*	—	—	[Henry et al., APL 2019]
TiN (150 nm) **_HZO (20 nm)_** _TiN (150 nm)_	ALD, 550 °C, 30 s	**300 K:** 11.5 µC/cm² @ 1.5 MV/cm f_{PUND} = 10 kHz	**100 K:** 10 µC/cm² @ 1.5 MV/cm f_{PUND} = 10 kHz	**100 K:** ~ 0.8 MV/cm *(symmetric dev.)*	**300 K:** > 10⁹ cycles @ 2 V$_p$ / 100 kHz	**100 K:** > 10⁹ cycles @ 2 V$_p$ / 100 kHz	[Wang et al., Jpn J Appl Phys 2019]
_Pt (50 nm)_ _TiN (10 nm)_ **_Si-HfO₂ (10 nm)_** _TiN (10 nm)_	ALD, 800 °C, 20 s	**300 K:** ~ 38 µC/cm² @ 4 MV/cm	**100 K:** ~ 47 µC/cm² @ 4MV/cm	**100 K:** ~ 1.38 MV/cm *(symmetric dev.)*	**300 K:** > 3 × 10⁷ cycles @ 4.5 V$_p$ / 100 kHz	—	[Zhou et al., Acta Mater. 2015]

* In the current work row, applied PUND voltage was converted into electric field as $E = V_p/(d_{HZO}+d_{Al2O3})$, taking into account the drop over the entire HZO+Al₂O₃ stack of 11.3 nm.

2.2.5 Analog operation

For efficient online training in in-memory-computing (IMC) architectures, one essential condition for the synaptic weight element is linearity and symmetry of conductance states upon application of a train of programming pulses of either identical magnitude and width or increasing and decreasing amplitude and width. Previously, it has been shown that multiple stable conductance states can be obtained at 5 K temperature in perovskite tunnel junctions. [44] Linearity of conductance can also be achieved by using more than one memory element as the synaptic weights, for example, by using a 1-transistor - 2-resistor (1T2R) structure. However, these additional circuit components bring the obvious effect of increased synaptic area overhead and design complexity. [45] In FTJ or FeFETs, linear modulation of conductance is a result of gradual rotation of the polarized FE domains [46-48] that can be controlled with pulse amplitudes, widths, by modification of gate stack and by changing ferroelectric crystallinity and grain size. [49, 50]

In **Figure 8**, we show that operation temperature is one additional parameter for controlling the linearity and symmetry of multiple polarization states in ferroelectric HZO devices, that can result in analog control of FeFET channel conductance. For the measurements of potentiation (increasing) and depression (decreasing) sides, increasing or decreasing amplitudes of pulsed voltages were used. The

amplitude range and voltage steps are specified in each panel since based on temperature range, the applied voltage ranges changed. It is found that with increasing pulse amplitude, there is a certain threshold value above which the polarization rotation is more pronounced leading to an almost exponential nature for increase in polarization. In the temperature range of 200 – 300 K, this gave rise of highly nonlinear increase and decrease of intermediate states. However, below 200 K, a sharp drop in nonlinearity is seen for all different frequencies, especially for 5 and 25 kHz. The non-linearity factor showed a minima at around 100 K for 5 and 25 kHz frequencies, showing almost an ideal situation for linear and symmetric synaptic weight update. Below 100 K, the linearity starts to deviate slightly again from the ideal value, however remaining more linear compared to high temperature responses.
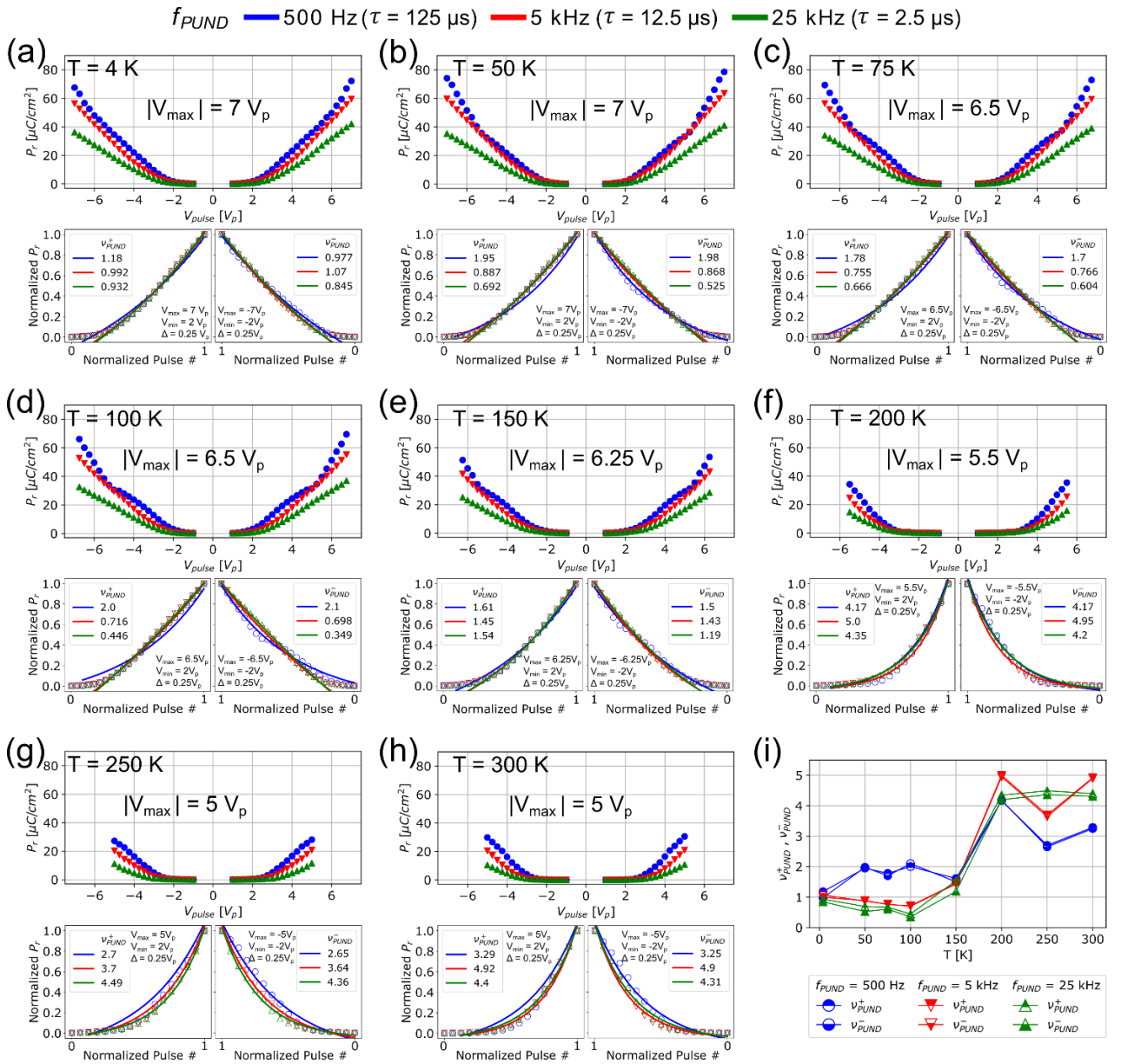

Figure 8. Intermediate state programmability analysis inferred from PUND polarization-pulse amplitude dependences at different frequencies from 300 K down to 4 K: The polarization-pulse amplitude *P-V* characteristics

are shown for f_{PUND} = 500 Hz (blue), 5 kHz (red), and 25 kHz (green) in the top panels, measured **(a)** 4 K, **(b)** 50 K, **(c)** 75 K, **(d)** 100 K, **(e)** 150K, **(f)** 200 K, **(g)** 250 K and **(h)** 300 K. The maximum pulse amplitude close to the critical breakdown voltage is indicated for each temperature. The respective bottom panels show the normalized polarization as a function of normalized pulse amplitude for the positive (negative) pulse amplitudes on the left (right). The corresponding maximum (minimum) pulse voltages V_{max} (V_{min}) are shown in the insects. The non-linearity factors for the positive (negative) pulses $v_{PUND}^{+}(v_{PUND}^{-})$, obtained from the fitting (see the text) are given for each temperature in the insets. **(i)** Temperature dependence of v_{PUND}^{+} and v_{PUND}^{-} which mimic the potentiation and depression non-linearity factors. v_{PUND}^{+} and v_{PUND}^{-} are found to be very similar throughout the temperature range from 300 K down to 4 K. The overall non-linearity at cryogenic temperatures is significantly reduced as compared to 300 K data, with the minimal non-linearity range between approximately 4 K and 100 K. All devices were measured from the same die coming from a 150 mm wafer. To avoid the fatigue effects (among others), for each temperature point, an individual device was measured.

From experimental data of **Figure 8**, the linearity factor has been calculated using the formula, $P_{norm} = A + B(1 - e^{\left(v_{PUND}^{+(-)} V_{norm}\right)})$, where P_{norm} is the normalized P_r, A and B the fitting constants, $v_{PUND}^{+(-)}$ is the PUND-measurement non-linearity coefficient of polarization update for the positive and negative pulse amplitudes respectively, and V_{norm} is the normalized pulse amplitude. $v_{PUND}^{+(-)}$ mimic the potentiation and depression synaptic weight update non-linearity factor, n. [51] For $n = 0$, the response is perfectly linear. For real synaptic devices, the n values were demonstrated in the range of $v \approx 2$–5 at room temperature. [52] For the present HZO sample, the v value is found to be on the higher side of this range at higher temperature, however much improved v value below 100 K indicate well-controlled domain rotation in our devices leading to the possibility of excellent analog operation at or below 100 K. The non-linearity values for the potentiation (v^{+}_{PUND}) and depression (v^{-}_{PUND}) side for each temperature is shown in the plots. Both potentiation and depression non-linearity are found close to each other showing very high symmetry of analog states for synaptic potentiation and depression side. These results indicate that at or below 100 K, the ferroelectric domain rotation in HZO is most gradual, especially with higher frequency electrical pulses (**Fig. 8 (a - d)**) and it is easier to obtain large number of analog states for online training in IMC architectures.

3. Conclusion

We reported on fabrication, structural and 4 - 300 K electrical characterization of ferroelectric HZO devices. The films grown by plasma-enhanced atomic layer deposition on TiN bottom electrodes, provided a large in-plane tensile stress on the HZO films, stabilizing its polar orthorhombic phase. This makes it possible to operate the devices to have a large open hysteresis with P_r values of > 30 µC/cm^2 at room temperature, even without any wake-up cycles. Upon cooling down, an overall increase in P_r value occurred showing a maximum at around 100 K and eventually showing similar

P_r at 4 K, however, the switching became more gradual at cryogenic temperatures, leading to the possibility for more precise control of analog states. Another interesting feature is that the leakage current component of the HZO capacitors reduce significantly when measured at 100 K or below, providing a significant improvement in imprint, fatigue and breakdown effects. Our work shows that ferroelectric technology has potential for cryogenic memory applications, *e.g.*, in the context of high-performance computing, space technologies and quantum information processing.

4. Experimental Section/Methods

Fabrication: The TiN/HZO/Al$_2$O$_3$/Au (MFIM) capacitors were fabricated with the bottom electrode TiN being grown using plasma-enhanced atomic layer deposition (PEALD) and the HZO layer using thermal atomic layer deposition (ALD). TiN (HZO) thickness was 30 (10) nm. For the MFIM device stacks, the TiN bottom electrode (BE) was fabricated on Si wafers with 500 nm thermally grown SiO$_2$ on top by using PEALD (SUNALE R-200 Advanced, Picosun). TiCl$_4$ and ammonia were used as precursors for TiN growth, where nitrogen was used as carrier and purging gas, and argon flow was used for plasma. The growth process was performed at 420 ^{o}C. HZO film was deposited at 200 ^{o}C on with tetrakis (dimethylamino)hafnium (TDMA–Hf) and tetrakis (dimethylamino)zirconium (TDMA–Zr) as the Hf and Zr precursors, respectively, and water (H$_2$O) as the oxidant. Nominally optimized 50:50 ratio of the Hf:Zr was obtained using one cycle of TDMAH and H$_2$O followed by a cycle of TDMAZ and H$_2$O. The thickness of the TiN layer was calibrated with cross-sectional SEM while HZO thickness was calibrated using profilometry. Thicknesses of the film varied slightly from the targeted thickness. For instance, 1200 cycles of TiN resulted in thicknesses of 31 nm and 54 supercycles of HZO resulted in nearly 9.8 nm HZO. Right after the deposition of HZO, 1.2 nm Al$_2$O$_3$ was deposited at 200 ^{0}C without breaking vacuum. Following the film deposition, rapid thermal annealing (RTA) step was done for 30 sec at annealing temperature of 500 ^{0}C under nitrogen atmosphere. After RTA, Au top electrodes were deposited as the TE via thermal evaporation device to complete the capacitors with different sizes of 100 μm × 100 μm, 200 μm × 200 μm and 500 μm × 500 μm.

Characterization: The structural characterization was done using X-ray reflectivity (XRR), out-of-plane grazing-incidence X-ray diffraction (GIXRD) and scanning transmission electron microscopy (STEM). For XRR/GIXRD, we used a Rigaku SmartLab diffractometer operating at 45 kV, 150 mA, with a Cu rotating anode. In both cases, we used a divergence slit of 0.1º, a 5º Soller slit in the incident side, and a parallel beam geometry. For XRR, we used a double-bounce Ge(220) monochromator and a 5º Soller slit on the receiving side. For GIXRD we used no monochromator and a parallel-slit analyzer with a resolution of 0.114 º on the recieving side. The GIXRD measurements were taken

with an incident angle ω = 0.38º. STEM measurements were performed using a Cs-corrected JEOL JEM-2200FS at 200 keV. The wedge-lamellas were prepared by focused ion-beam with a JEOL JIB-4700F at 30 kV, with an estimated lamella thickness of 30 nm at the scanning location. All electrical characterizations were done using a commercial transimpedance amplifier (*I-V* converter), and an arbitrary waveform generator outputting various waveforms and triggering a digitizing oscilloscope for data acquisition. A cryogenic probe station is used for varying temperatures between 4 K – 300 K.

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Supplementary information: Ferroelectric $Hf_{0.5}Zr_{0.5}O_2$ for Analog Memory and In-Memory Computing Applications down to Deep Cryogenic Temperatures

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Table S1. Structural Characterization Data. Lattice parameters fitted for the crystallographic phases present in the Si/HZO and TiN/HZO

Stack	Lattice System	Space Group	a (Å)	b (Å)	c (Å)	β (º)
Si/HZO	(HZO) Monoclinic	$P2_1/c$	5.11	5.15	5.27	98.06
Si/HZO	(HZO) Tetragonal	$P4_2/nmc$	3.57	3.57	5.19	90
TiN/HZO	(HZO) Tetragonal	$P4_2/nmc$	3.57	3.57	4.99	90
TiN/HZO	(HZO) Orthorhombic	$Pca2_1$	4.96	5.05	5.06	90
TiN/HZO	(TiN) Cubic	$Fm\overline{3}m$	4.20	4.20	4.20	90

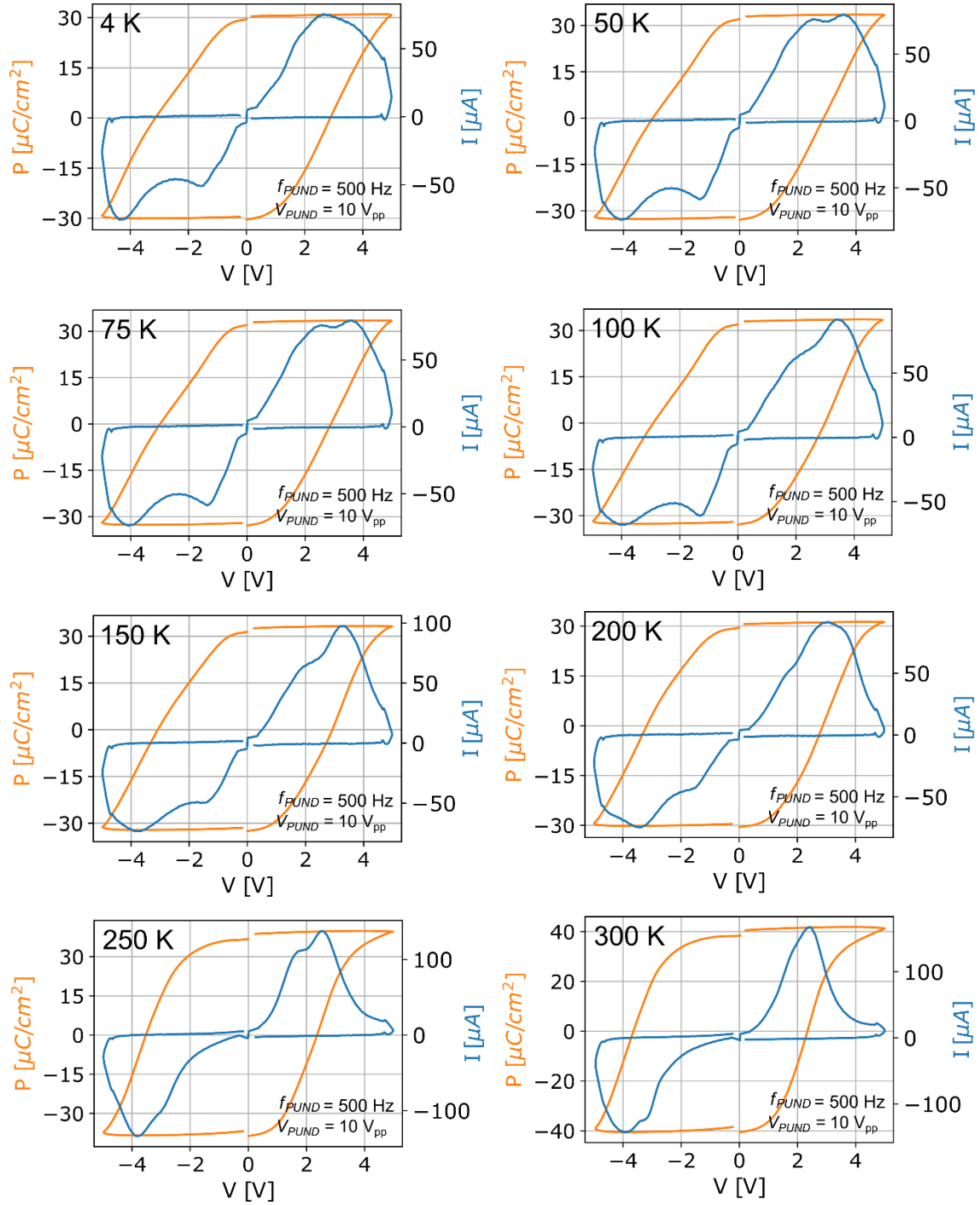## S1. Electrical Characterization Data showing Pristine Device Performance

Figure S1: Polarization- voltage and current-voltage characteristics from wake-up-free pristine junctions measured between 300 K and 4 K: *I-V* (blue) and *P-V* (orange) characteristics of the pristine HZO capacitors measured with PUND sequence using $V_{PUND} = 10$ V$_{pp}$ at $f_{PUND} = 500$ Hz without pre-pulsing. The data show polarization and current waveforms at low temperature (< 200 K) almost identical to the data showed in the main text where 5×10^3 PUND pulses at $V_{PUND} = 10$ V$_{pp}$ at $f_{PUND} = 500$ Hz were applied prior to measurements within the temperature range 4 K – 200 K. Between 200 K and 300 K, while initially showing higher P_r values, 250 K – 300 K data in the main text were acquired after 5×10^3 PUND pulses at $V_{PUND} = 9$ V$_{pp}$ at $f_{PUND} = 500$ Hz to stabilize the P_r from dropping down and enable the frequency and amplitude dependence studies.

S2. Electrical Characterization Data showing device-to-device variations at different temperatures and frequencies from the same chip.
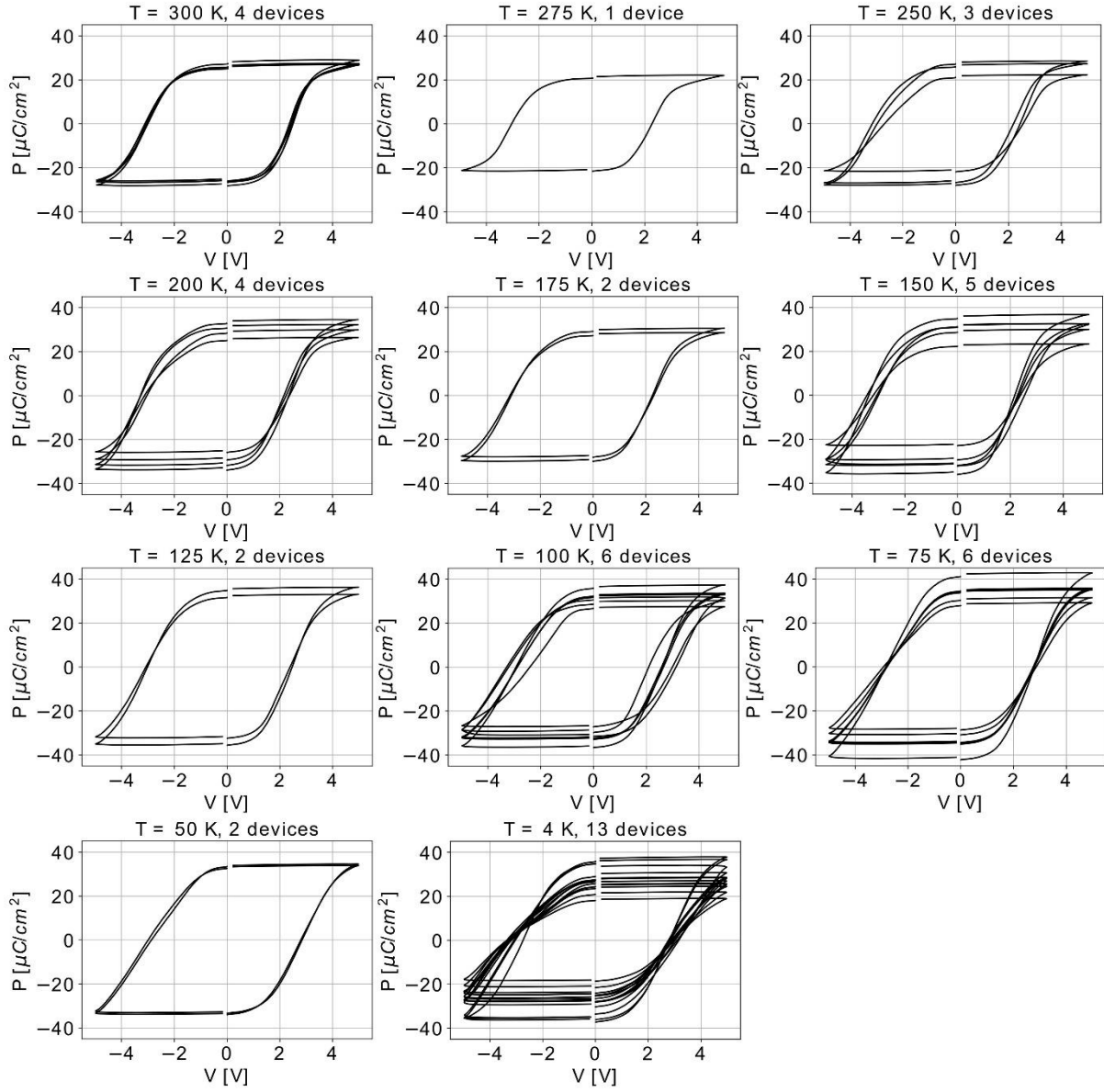

Figure S2. P-V data from one single chip (chip L) showing device to device variation of critical parameters (Pr, Vc and MW) at all temperatures.
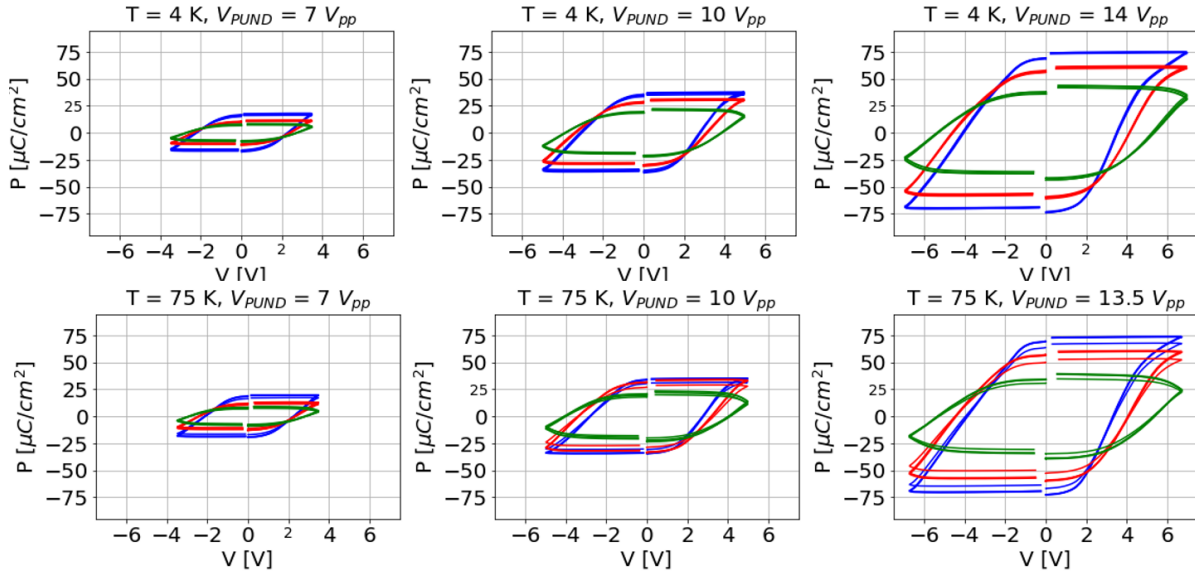
Figure S3. Electrical Characterization Data showing device-to-device variations at 4K and 75 K at 3 different frequencies for multiple devices.
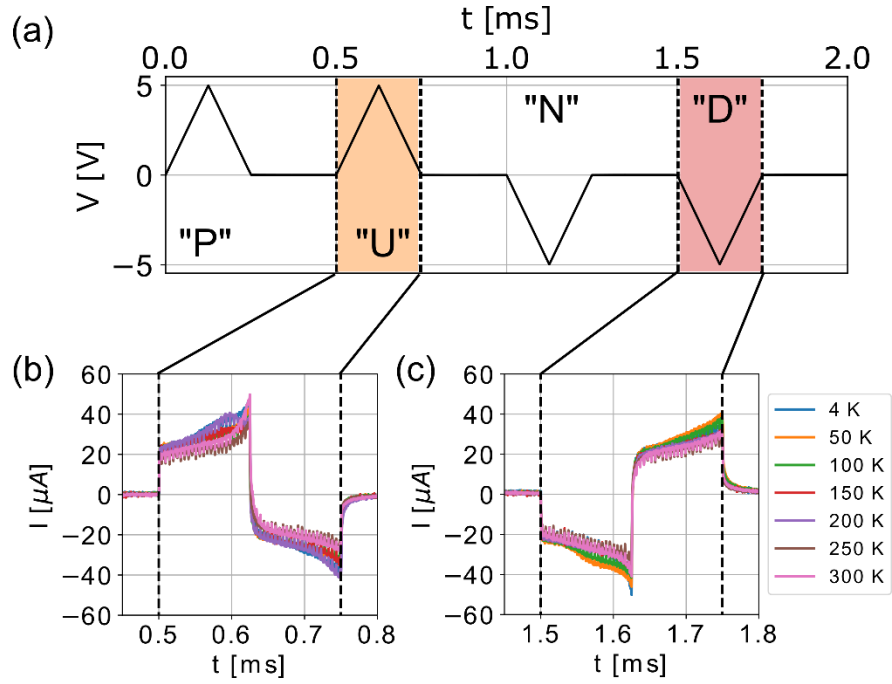

Figure S4. Leakage current comparison of the HZO capacitors at 300, 250, 200, 150, 100, 75 and 4K (taken from raw I-V data from the second PUND pulse (U and D), not showing the ferroelectric current contribution of the PUND).
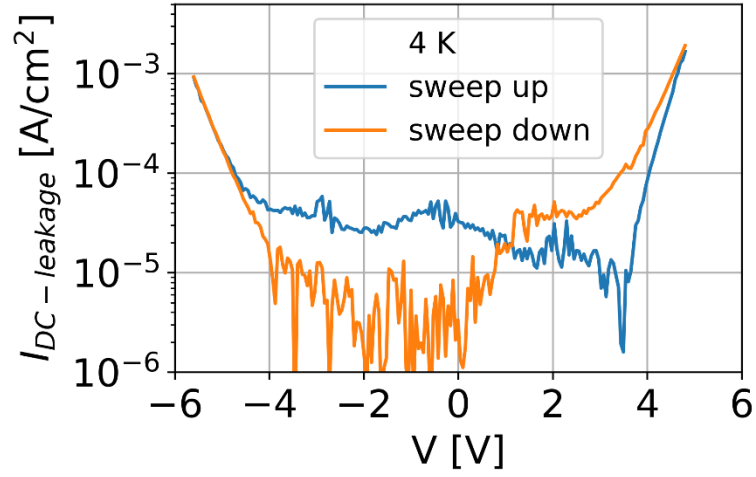
Figure S5. DC I-V of the HZO capacitors showing quasi-static leakage current at 4K.
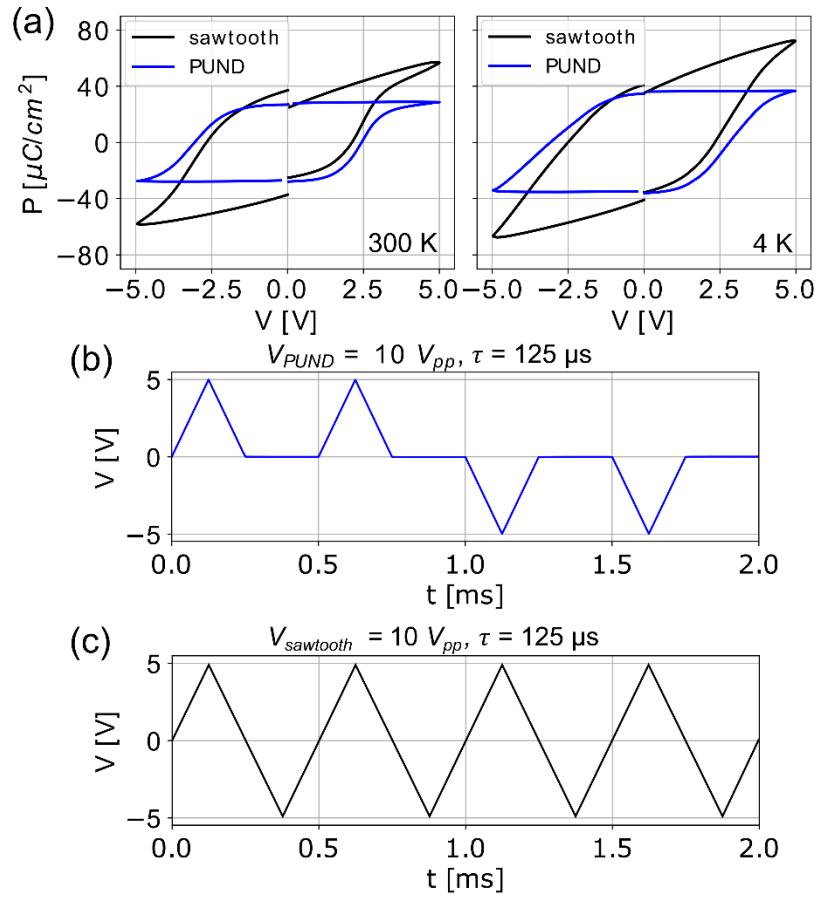

Figure S6: P-V plot with and without leakage subtraction at 300 K and 4 K and the corresponding pulse waveforms used to measure the two responses (b) PUND and (c) sawtooth.
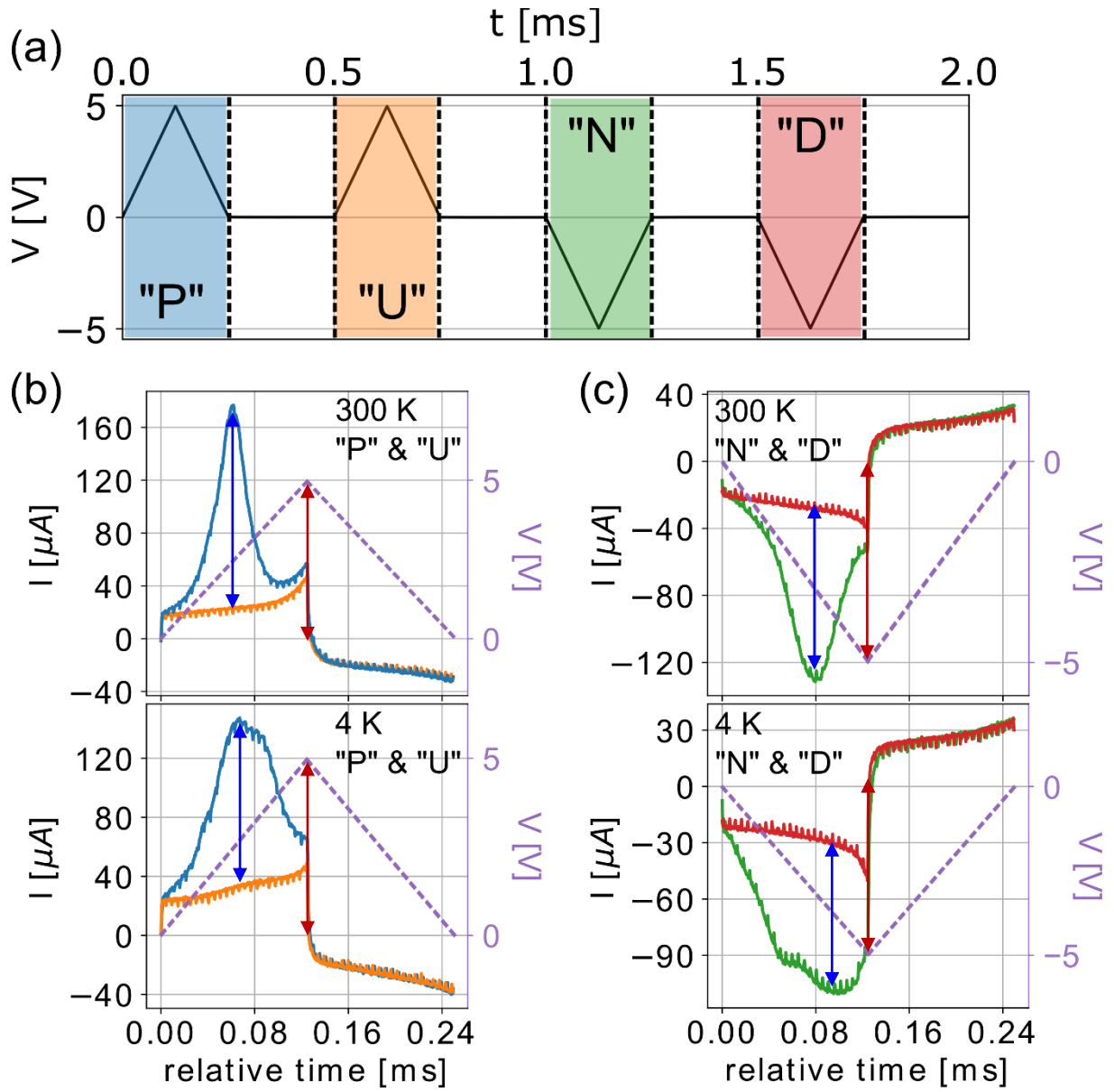
Figure S7. Figure with first pulse and second pulse current response on top of each other (from I-t curves: (P (blue) on top of U (orange) and N (green) on top of D (red)) together with the voltage pulse showing the displacement current contribution (represented by the blue arrow) and at highest voltage (tip of the triangle), the displacement current is zero (represented by the red arrow).

Table S2. Leakage Current comparison with multiple different HZO capacitors with varying metal electrodes, stack compositions and deposition and annealing conditions.

Device	Anneal temp.	Leakage current density	Ref.
TiN/Hf$_{0.5}$Zr$_{0.5}$O$_2$/TiN	800 °C for 30s in N$_2$	8x10^{-5}A/cm^2 @-2V	[1]
TiN/Al$_2$O$_3$/ Hf$_{0.5}$Zr$_{0.5}$O$_2$/TiN	800 °C for 30s in N$_2$	5x10^{-5}A/cm^2 @-2V	[1]
TiN/Hf$_{0.5}$Zr$_{0.5}$O$_2$/ Al$_2$O$_3$/TiN	800 °C for 30s in N$_2$	7x10^{-5}A/cm^2 @-2V	[1]
W/HZO/W	700 °C for 5s in N$_2$	1.2x10^{-3}A/cm^2 @-2V	[2]
W/Pt/HZO/W	700 °C for 5s in N$_2$	6x10^{-5}A/cm^2 @-2V	[2]
W/Pt/HZO/Pt/W	700 °C for 5s in N$_2$	1x10^{-5}A/cm^2 @-2V	[2]
Ti/HZO/Ti	450 °C for 30 s in N$_2$	10^{-3}A/cm^2 @-2V	[3]
Ti/HZO/Ta	450 °C for 30 s in N$_2$	10^{-3}A/cm^2 @-2V	[3]
Ti/HZO/Pt	450 °C for 30 s in N$_2$	3x10^{-5}A/cm^2 @-2V	[3]
TiN/HZO/TiN	700 °C for 30 s in N$_2$	3x10^{-3}A/cm^2 @-2V	[4]
TiN/HZO/Al$_2$O$_3$/Au	500 °C for 30 s in N$_2$	1.2 x10^{-4}A/cm^2 @-2V (300 K) 10^{-5} A/cm^2 @-2V (4 K)	This work

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