

Memristor-based Reconfigurable True Time Delay Circuit

Fan Yang, *Student Member, IEEE*, Alexander Serb, *Senior Member, IEEE*, Shiwei Wang, *Senior Member, IEEE*, Christos Papavassiliou, *Senior Member, IEEE*, Themistoklis Prodromakis, *Senior Member, IEEE*,

Abstract—A Memristor-controlled CMOS reconfigurable true time delay circuit is introduced in this paper. The delay circuit includes 3 stages of g_m -C all pass filter delay elements connected in cascade, and memristor-based tuneable DC voltage sources. The memristor value variation changes the DC bias voltage inputs of the delay elements, and thus controls the delay time indirectly: The memristor resistance changes in analogue from $10\text{k}\Omega$ to $17\text{k}\Omega$, changing the tuneable DC voltage source output from 584mV to 711mV DC voltage and the delay from 269ps to 632ps . The delay circuit can work in a frequency range from 50MHz to 1.6GHz with gain ripple smaller than 3dB . The resolvable delay time step across the delay range is $<8.7\text{ps}$, troughing at as low as 0.4ps . A delay circuit working in the MHz region is also designed to compare the performance with the GHz circuit, and a memristor programming circuit is built to change the resistance levels of memristors.

Index Terms—Memristor, RRAM, CMOS, time delay, analogue, RF.

I. INTRODUCTION

WITH the fast development of information transmission around the world, communication systems with less power, higher bandwidth and smaller signal distortion are needed. The phased array antenna system is a widely used communication technology capable of fast steering multiple beams in different directions with high signal to noise (SNR) ratio[1][2]. It also has high reliability as the failure of some array components will not strongly reduce the performance of the whole array system[3]. In phased array systems, true time delay (TTD) elements are the key components[4]. True time delay can be used in the sub-array level of the array system to alter the beam of radio wave direction, and reduce the "beam squint" phenomenon[5] [6].

The true time delay needs to be reconfigurable to steer the phase array system. There are many ways to achieve it, including using switched transmission lines[6][7][8], inductor or capacitor network[9][10], microelectromechanical (MEMS) devices[11], and complementary metal-oxide semiconductor (CMOS) technology combined with other controlling signals[12][13][14][15][16][17]. In these methods, CMOS technology is the most suitable one for on-chip integration

and combines with other techniques. A component called memristor can be considered when combining with CMOS technology. The memristor, also called resistive random-access memory (RRAM), is a two terminal non-volatile electronic device[18]. The resistance of a memristor component depends on the history of voltage or current on it, thus the resistance value of the memristor can be controlled by voltage or current signal[19]. Broadly, there are two kinds of memristor devices, one can change its resistance between two digital stages high and low [20], and another one can change its resistance continuously in an analogue way[21][22]. In the case of analogue memristor, the memristor device can be seen as a finely tuneable resistor. Memristors have shown good potential in different research area, especially in artificial neural networks[23] and as memory devices[24]. However, the analogue memristor can also be used in reconfigurable analogue circuit design. By controlling the memristor's resistance value, the characteristics of the circuit output can also be adjusted.

The biggest problem that limits the application of multi-stage analogue memristors in high-frequency circuits is the parasitic capacitance in the memristor device. As the structure of a metal-oxide-metal memristor is similar to a metal-insulator-metal(MIM) capacitor, the memristor also has an unwanted capacitance in between its two metal layers. The parasitic capacitance value depends on the size, material and technology of the memristor. For a $10\times 10\mu\text{m}^2$ metal-oxide memristor, the parasitic capacitance can be around 10pF [25], which is a very large value for RF applications. This research aims to apply multi-stage memristors in radio frequency reconfigurable designs. To deal with the influence of the parasitic capacitance in the memristor, this research applies memristors in low-frequency voltage generators, and then uses the tuneable voltage generators to control a radio frequency device. By doing that, the memristor can control a high-frequency device without affecting the high-frequency signals.

In this research, a tuneable true-delay circuit that uses memristor-CMOS hybrid circuitry for fine delay tuning is proposed. The output voltage value of the DC source is decided by the memristor resistance level, and the delay time of the delay element is adjusted by its input DC voltage. In this case, the memristors control the delay time of the circuit indirectly. In section II, the schematic of the memristor-based DC voltage source and delay element are reviewed. A 3-stage tuneable delay circuit works in GHz is designed based on the tuneable voltage source and delay element to increase the range of achievable delays to $[155, 364]\text{deg}$ at 1.6GHz . A

F. Yang, A. Serb, S. Wang and T. Prodromakis are with the Centre for Electronics Frontiers, Institute for Integrated Micro and Nano Systems, University of Edinburgh, Edinburgh, EH9 3BF, UK. (Email: fan.yang, aserb, shiwei.wang, t.prodromakis@ed.ac.uk)

C. Papavassiliou is with the Department of Electric and Electronic Engineering, Imperial College London, London, SW7 2AZ, UK. (Email: c.papavas@imperial.ac.uk)

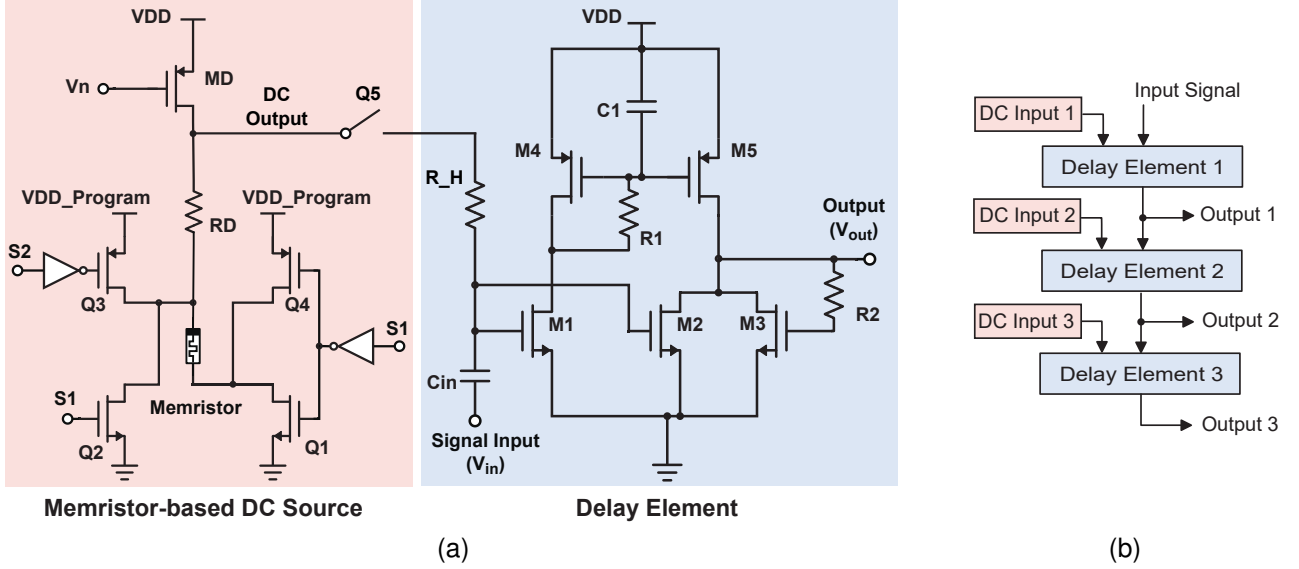


Fig. 1. (a) Schematic of the memristor-controlled DC voltage source (red region) and delay element (blue region). In the DC voltage source, MD , RD and the memristor form the normal DC voltage source part, and transistors $Q1$ to $Q4$ control the memristor programming. (b) Structure of the cascade 3-stage delay circuit. The circuit includes three tunable DC sources and three delay elements, with three output ports that have different delay ranges.

memristor programming controller is designed to change the memristor resistance level based on digital commands, and a lower frequency delay circuit working in the MHz region is also designed to compare with the GHz circuit. The section III records the simulation data of the memristor-based DC source, the GHz tuneable delay circuit and the MHz delay circuit. The comparison results of the delay circuits with other works are recorded in the section IV. The section V concludes this research and discusses further prospects.

II. THE DESIGN AND METHODOLOGY

A. Basic Delay Element Overview

An ideal delay element can be seen as an all-pass filter with gain $G=1$ [26][27][28]. A CMOS all-pass filter was discussed in literature [29]. It uses a reconfigurable capacitor group to control the output delay time ($C1$ in Fig. 1a). By connecting and combining different capacitors in the reconfigurable capacitor group, the output delay time can be adjusted. However, limited by the number of capacitors, the minimum step of delay time is large, and the necessary space for the integration of capacitors is also large. In this research, the basic delay element schematic remains the same, but the output delay is adjusted via the input gate voltage of the NMOS transistors $M1$ and $M2$, as shown in Fig. 1a. The red region is a memristor-based tuneable DC source, and the blue region is the delay element.

In the delay element, NMOS transistors $M1$ to $M3$ have the same width and length, while the width of PMOS transistor $M5$ is twice that of the width of $M4$. The gain function of the delay element is shown below, in which gm_1 to gm_4 are the transconductance of transistors $M1$ to $M4$, $I_{D(M5)}$ is the current through $M5$, C is the capacitance of the capacitor $C1$. The current through $M5$ is two times the current through $M4$ and equals the sum of the currents on $M2$ and $M3$. The

currents on $M1$ to $M3$ are ideally the same. In this case, $M1$ to $M3$ have the same transconductance, and $M5$ has two times the transconductance of $M4$. Equation 1 shows the gain function of the delay element is that of an all-pass filter when $gm_1=gm_2=gm_3$. The delay time offered by the circuit relates to frequency: At low frequency, the delay is approximately the time constant of the all-pass filter, as shown in equation 2, where $d\phi$ is the phase shift, $d\omega$ is the change in frequency, and D is the delay time at the output. For high-frequency condition, the delay starts to reduce fast when the frequency approaches the pole of equation 2, and reduces to half of the maximum delay value at the frequency pole. The functions shown in equations 1 to 2 are the basic functions of the circuit as an all-pass filter. To expand the working frequency range of the delay element, resistors $R1$ and $R2$ are added in the circuit as shown in Fig 1a. Resistor $R1$ helps increase the output phase linearity by creating an inductive peak at the cut-off frequency similar to the nulling resistor in OpAmp[30], and resistor $R2$ combines with the parasitic capacitance at the output port acts as an active inductor which expands the bandwidth[29][31].

$$H(s) = \frac{V_{out}}{V_{in}} = \frac{2gm_1}{gm_3 \times (1 + \frac{sC}{gm_4})} - \frac{gm_2}{gm_3} \quad (1a)$$

$$= \frac{1 - s\frac{C}{gm_4}}{1 + s\frac{C}{gm_4}} \quad (1b)$$

$$D = \frac{d\phi}{d\omega} = \frac{\frac{2C}{gm_4}}{1 + (\frac{2\pi fC}{gm_4})^2} \approx \frac{2C}{gm_4} \quad (2)$$

$$gm_4 = \sqrt{\beta_1\beta_4} \times (V_{in} - V_{T1}) = \sqrt{\beta_1\beta_4} \times V_{OV1} \quad (3)$$

$$\frac{dD}{dV_{OV1}} \approx \frac{-2C}{\sqrt{\beta_1\beta_4} \times V_{OV1}^2} \quad (4)$$

In this research, the input DC voltage of transistor M1 V_{in} is used to (indirectly) control g_{m4} . Equation 3 is the relationship between V_{in} and g_{m4} . β_1, β_4 are the gain factors of the M1 and M4, V_{T1} is the threshold voltage of M1, and V_{OV1} is the overdrive voltage of M1. Based on equation 1 2 and 3, V_{in} can then control the gain and delay of the circuit. With larger V_{in} , the delay at the output will be smaller. When V_{in} close to the V_{T1} of the transistor, the delay is larger, and the delay variation with the change of V_{in} also becomes larger. Equation 4 is the derivative equation of delay time D and overdrive voltage V_{OV1} , shows that at low frequency, when V_{OV1} is close to 0, the trend of delay variation becomes very huge.

The delay elements can be cascaded to get a larger delay range. Fig 1b shows a 3-stage delay circuit. The number of stages the circuit can include is decided by the required gain variation range. Although connecting three 1st-order all-pass filters in series can not improve their performance as all-pass elements, this method is still a simple method for expanding the delay range. A problem is, that a circuit can never form an ideal all-pass filter, as there are always errors between its poles and zeros. Cascading three all-pass elements that are the same makes the error grow exponentially. To deal with it, the input DC voltages of the three all-pass stages can be set slightly differently, hence the errors in the three stages can counteract each other.

With more stages of delay element, the output delay range is expanded, but the gain variation range is also larger and the minimum delay at the end of the cascade also accumulates. The DC input offered by the memristor-based DC sources lies in a voltage range larger than the threshold voltage of the transistors. As we seek to maintain the gain variation to $< \pm 3$ dB, the voltage range of the DC input will also be limited by the output gain variation. To improve the minimum delay step of the delay circuit, each stage of the delay element combines with a memristor-based DC source to control the input DC voltage. The 3-stage delay circuit has three output ports, Output 1, 2 and 3, corresponding to the different output delay ranges. The minimum delay offered by the whole delay circuit is in Output 1, with DC input 1 set to the maximum value; The maximum delay is in Output 3, when all the DC inputs are set to the minimum value.

B. Memristor-Controlled Tuneable DC Source with Memristor Programming Interface

The red region in Fig 1a is the memristor-based DC source. Transistors $Q1$ to $Q4$ are the programming circuit, resistor RD , transistor MD and memristor form a DC voltage source. Transistor $Q5$ is a switch which turns off when the memristor is in programming. R_H is a resistor with very high resistance to avoid AC signal flows into the DC source. The delay circuit works with a voltage supply of 1.8V. However, based on technological reasons the memristor in this research needs a 5V pulse for programming. In this case, only the transistors in the DC source (MD and $Q1 - Q5$) and memristor digital programming controller are high-voltage MOSFETs which are suitable for working with 5V power supply. The whole circuit

TABLE I
MEMRISTOR-BASED DC SOURCE WORKING MODES WITH DIFFERENT INPUT CONTROL SIGNALS

Working Mode	Signal S1	Signal S2
Normal work	Low	Low
Programming (up to down)	Low	High
Programming (down to up)	High	Low

can work with all transistors at the same voltage rate if the memristor is capable of programming at low voltage.

When the DC source is in normal work, V_n is set to a specific value to turn on transistor MD , and $VDD_{Program}$ is set to 0V. Transistors $Q1, Q5$ opens, $Q2$ to $Q4$ close. As the resistance of $Q1$ in the open state is very small, in this case the voltage output is decided by the ratio between the resistance of transistor MD and the resistance of $[RD + \text{Memristor}]$. To program the memristor, V_n will first be set to 5V to turn off PMOS MD , then $VDD_{Program}$ set to pulse signal with peak value around 5V. Program the memristor from direction up to down needs $Q1, Q3$ open, and $Q2, Q4$ close. Program the memristor down to up will need $Q2, Q4$ open and $Q1, Q3$ down. The four transistors $Q1$ to $Q4$ are controlled by programming signals S1 and S2. Table I shows the relationship between the working mode of the DC source and the signal S1, S2. It can be found that in default condition both S1 and S2 are set to low voltage level, and the DC source is in normal work mode. To program the memristor, depending on the programming direction, S1 or S2 is set to high voltage level. In up-to-down programming mode, the output of the DC source offers a high DC voltage to the input of the delay element, reducing gain and increasing power dissipation. To avoid this situation, a specific programming procedure is followed: a) Shut down MD, which limits the current through MD route in programming, b) Shut down switch $Q5$. c) Proceed with programming.

C. Memristor Programming Controller

The block diagram of the memristor programming controller is shown in Fig 2. For the 3-stage delay circuit, 3 memristor-based DC sources are used. The programming controller controls activity at switches S1, S2 for all 3 stages, and programs a single memristor at a time. When the $VDD_{Program}$ ports of the memristor-based DC sources shown in Fig 1a are connected to the programming pulses, the chosen memristor can be programmed. Combined with the red region of Fig 1 (a), to program the three memristors separately, 3 groups of S1, S2 signals, in total 6 control signals are needed. The structure of the memristor programming controller can be divided into three layers, the bottom layer is a scan-chain configuration, while the bottom and middle register layers form a serial-to-parallel register configuration, and finally the third layer has 6 AND gates whose outputs connect to memristor-based DC sources.

The programming procedure begins by serially feeding the correct 6-number binary codes to the input register via Data In with a serial clock CLK. At the same time, Data Out starts to receive the Data In code from the output of the register F1_6 at

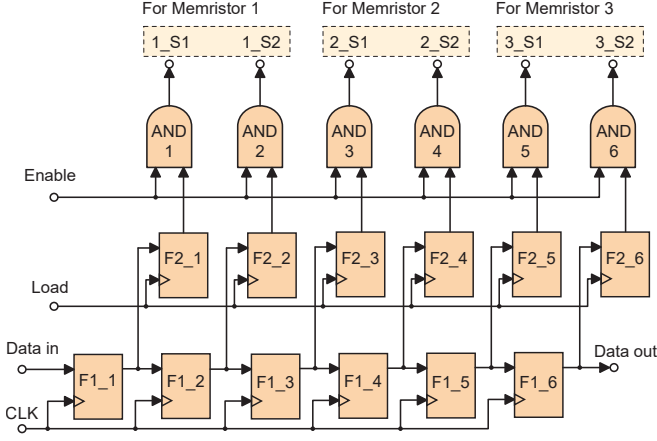


Fig. 2. The memristor digital programming controller. In one programming process, only one memristor should be programmed. Data In is the 6-bit programming command, and 6 output signals 1_S1 to 3_S2 are the control signals S1&S2 for the three memristor-based DC sources.

the sixth clock signal. Next, the Load signal rises and activates the serial-to-parallel register block. Thereafter, the first layer registers are reset to all-0 in the process. Finally, to control the timing of the bias, an asynchronous Enable signal is used. In the tuneable DC sources, the $VDD_{Program}$ port in Fig 1a offers pulse to the memristor, and MD , $Q5$ turn off. Once the programming of one memristor is finished, $VDD_{Program}$ is set to 0V first to reset the voltage at the DC Output node and then the Enable signal closes.

D. Memristor-Controlled GHz / MHz tuneable Delay Circuit Block Diagram

The block diagram of the whole circuit is shown in Fig 3. The delay circuit includes both a 3-stage delay element part that works in low GHz and a 3-stage delay element part works in MHz. This is to research the performance of the delay schematic in low-frequency application, and compare the performance of the low and high-frequency delay circuits. Both of the delay circuits use the same memristor-based DC sources group to get DC voltage inputs. DC1, DC2, DC3 are the outputs of the three tuneable DC sources, corresponding to the three input DC voltages of 3-stage delay circuits. To reduce the power consumption and avoid signal interference between different delay parts, the GHz delay part and MHz delay part will not work at the same time. Only one delay part can get the DC voltage from memristor-based DC sources, another delay part will be turned off. Furthermore, a GHz oscillator and a MHz oscillator are designed as signal generators for the two delay parts. The frequency of their output signal can be adjusted in a small range, and the center frequency of the two oscillators are 1.6GHz and 10MHz. The memristor programming controller connects to the three tuneable DC sources as shown in section II-C. The whole circuit is integrated on chip in the area of $1mm^2$, which will be shown in the section III.

III. SIMULATION RESULTS

All simulations of the memristor-based tuneable delay in this section were performed at post-layout. Delay data was

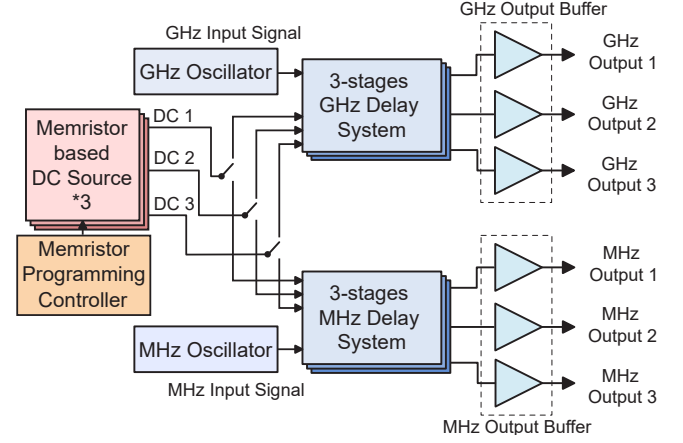


Fig. 3. Block diagram of the whole circuit. The whole tuneable delay circuit includes a GHz delay circuit with output buffers, an MHz delay circuit with output buffers, three memristor-based DC sources, a memristor programming controller, and two oscillators for input signal generation.

simulated at the outer pins of the corresponding pads (i.e. including pad ring effects). The memristor model used in this research offers a $10k\Omega$ to $17k\Omega$ resistance range. This resistance range is small compared with other RRAM models, but it is sufficient to support a good delay range, as shown below. The minimum step for memristor resistance variation is approximated at 1% of the current resistance value [32].

Simulation results of the GHz delay circuit indicate a working range of up to 1.6GHz where gain remains within 3dB of nominal. We thus quote a working range of 50 MHz to 1.6GHz and show performance result plots in the [0.05, 2]GHz frequency range.

A. Results of Memristor-based DC Source

The voltage output of a memristor-based DC source is shown in Table II. It can be found that the DC voltage output increases with the memristor resistance nearly linearly. We empirically find that to maintain the maximum gain variation from Output 1 to Output 3 of the delay circuit smaller than 3dB, the best input DC voltage range is around $600mV$ to $700mV$. Using $V_n=850mV$ our memristors support minimum and maximum output voltages of $584mV$ and $721mV$, with a tuneable voltage range of $137mV$. These voltage values also yield the maximum delay range of delay elements; it no accident that these voltages are close to the threshold voltage of $M1 - 2$. The V_n value is chosen based on the resistance range of the memristor, the value of resistor RD and the width/length ratio of transistor MD . To make sure the memristor value is constant during the delay working mode, the voltage on the memristor is maintained smaller than 0.6V. We note that V_n is an important tuning parameter: reducing V_n , the output voltage values are increased and the tuneable voltage range can also be expanded. Next, based on the minimum resistance variation step of the memristor, the resolution of the DC output can be inferred. Table II also shows the minimum voltage step of the DC source at different memristor values. The resolution data is calculated from the difference between the nominal output voltage (at the

TABLE II
OUTPUT VOLTAGE AND MINIMUM VOLTAGE STEP OF THE TUNEABLE DC
SOURCE AT DIFFERENT MEMRISTOR VALUE

Memristor(k Ω)	10	11	12	13	14	15	16	17
Voltage(mV)	584	607	629	651	670	688	705	721
Resolution(mV)	1.8	2.2	2	1.9	2.6	2.4	2.5	2.2

TABLE III
MONTE CARLO RESULT OF THE MINIMUM AND MAXIMUM VOLTAGE
OUTPUT OF THE DC SOURCE

	Mean	Max	Min	Std Dev
Min Output (mV)	594	841	432	123
Max Output (mV)	720	945	545	123

TABLE IV
CORNER, TEMPERATURE AND VOLTAGE SUPPLY VARIATION ANALYSIS OF
MEMRISTOR-BASED DC SOURCE.

Condition	Output Voltage (mV)
Normal ($V_n = 850\text{mV}$)	588 ~ 721
ff	953 ~ 1107
ff ($V_n = 942\text{mV}$)	590 ~ 727
ss	291 ~ 366
ss ($V_n = 752\text{mV}$)	590 ~ 720
T: -20°C	430 ~ 539
T: -20°C ($V_n = 810\text{mV}$)	589 ~ 719
T: 85°C	760 ~ 908
T: 85°C ($V_n = 900\text{mV}$)	591 ~ 727
VDD 1.7V	280 ~ 356
VDD 1.7V ($V_n = 749\text{mV}$)	588 ~ 721
VDD 1.9V	1009 ~ 1158
VDD 1.9V ($V_n = 950\text{mV}$)	591 ~ 725

chosen memristor value) and the output voltage at 101% of that memristor value. Simulated results show that with increasing memristor resistance the DC voltage output value increases. Voltage resolution remains $< 3\text{mV}$ for the whole memristor resistance range.

During simulation, the voltage on the memristor stays within the $[0.3, 0.5]\text{V}$ range, which will neither destroy the memristor element nor change its resistance level. When the memristor-based DC source switches to memristor programming mode, the programming pulse has a maximum theoretical peak value of 5V . The maximum current flowing through the memristor is 3.38mA with $V_{prog} = 5\text{V}$ and memristor value $10\text{k}\Omega$. In contrast, the current flow through the RD and MD is around $7\mu\text{A}$. The maximum voltage at the DC Output node of the DC source in programming mode (up to down) is around 2.5V , which will be cut off from sending to the input of the delay element by $Q5$.

The Monte Carlo simulation results of the minimum and maximum voltage outputs with memristor value at $10\text{k}\Omega$ and $17\text{k}\Omega$ are shown in Table III. Simulation results show the maximum and minimum voltage outputs may change in a fabricated integrated circuit, with the voltage tuneable range maintained between 104mV to 126mV . However, the tuneable DC source can adjust the output voltage range by

changing the gate voltage V_n of transistor MD in Fig 1a, hence this problem can be relieved in the measurement of the taped-out circuit.

The corner analysis results of the minimum and maximum voltage outputs with different transistor corners, different temperatures and different supply voltage V_{DD} are shown in Table IV. Transistor fast-fast (ff) and slow-slow (ss) are selected to be shown in the table. Temperature analysis chooses -20°C and 85°C as the minimum and maximum work temperature the device may face. The white regions of the table show the analysis results with the same V_n voltage in Fig 1a as a normal condition. Results show that the transistor corner and supply voltage variation significantly change the output voltage value, but the effect of temperature is comparatively small. This may be because the V_{ds} on transistor M_D in Fig 1a is strongly affected by the supply voltage and the transistor ff, ss corner effect. Also, the effect of corner, temperature, and voltage supply can be relieved by adjusting the gate voltage V_n . The green regions in Table IV show the output voltage range variations can be fixed by adjusting V_n .

B. Result of GHz Delay Elements

The width/length(W/L) of transistors $M1$ to $M4$ in the GHz delay elements are $20\mu\text{m}/180\text{nm}$, while the W/L of $M5$ is $40\mu\text{m}/180\text{nm}$, and the value of capacitance $C1$ is 33fF . The gain, phase and delay curves of GHz delay circuit Output 1 port with different memristor values are shown in Fig 4. The delay value reduces with increasing memristor resistance via higher input DC voltage in the delay circuit. The delay time changes with memristor resistance non-linearly. This is because the relationship between the delay and input DC voltage of the circuit is non-linear. Corresponding to equation 3 and 4, when the input voltage is small and close to the threshold voltage of the input transistor, the variation of the input voltage will cause a larger change in gm_4 and thus the final delay time. The gain and delay curves with high memristor value show an upward trend at $f > 1\text{GHz}$ as shown in Fig 4(c) (in fact peaking at approximately 2.2GHz , which is outside both our working and display ranges). The peaks are caused by the resistor $R1$ and $R2$ in Fig 1a, which expand the working frequency range (nulling resistor effect). Resistor $R1$ can make the phase curve more linear in low frequency. It causes a constant delay time reduction at low frequency, but has no influence on the delay time at a higher frequency close to the cut-off frequency of the curve, hence the difference between delay values at low and high frequencies is reduced. Resistor $R2$ combines with output capacitance and parasitic capacitance of the delay circuit and generates a peak at high frequency of the gain curve to expand the bandwidth of the delay element. The curve rising has a larger impact on the signal with higher input DC voltage.

The gain, phase and delay of the three output ports in the GHz delay circuit are shown in Fig 5, with the detailed data recorded in Table V. In a cascade circuit, the later stage circuits will have larger gain variations. The 3dB gain variation limit is not violated if the second and third stages of the delay circuit use memristors in range $[11, 16]\text{k}\Omega$, whilst the first stage delay

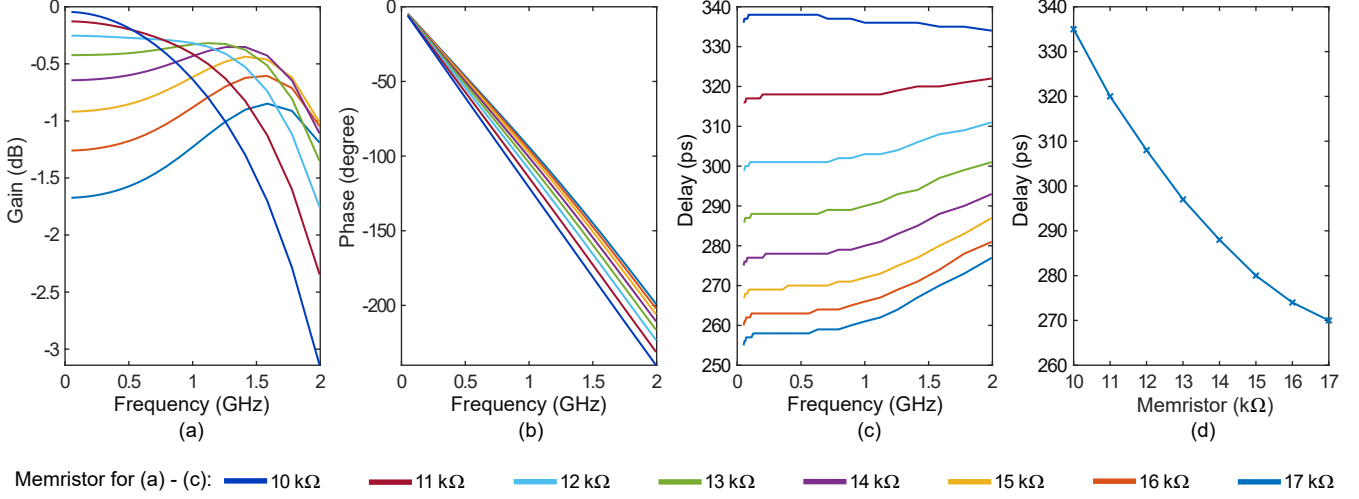


Fig. 4. (a) Gain, (b) phase and (c) delay time of the GHz delay circuit Output 1 port with different memristor value. The gain variation in Output 1 is $[-2.2, 0]$ dB in the range of $[0.05, 1.6]$ GHz. Delay range reduces when frequency increases. At 1.6GHz, the delay range offered by Output 1 is $[269, 335]$ ps. (d) The delay time with different memristor values at 1.6GHz.

uses full $[10, 17]$ kΩ resistance range. The working frequency range of the GHz delay circuit is 50MHz to 1.6GHz with gain variation smaller than 3dB. For gain values, the circuit should maintain the gain variation smaller than 3dB in all the working frequencies. To summarise, Table V records the gain variation from 50MHz to 1.6GHz of the cascade delay circuit, and the Phase and Delay data with different memristor values at 1.6GHz. At 1.6GHz, the GHz delay circuit can offer $269ps$ to $632ps$ delay time, which is 154° to 360° phase shift, with gain variation from 1dB to -2dB. The tuneable phase shift range at 1.6GHz is 206° . It can be observed from Fig 5 and Table V that there is a delay gap between $335ps$ and $373ps$, which is larger than the maximum delay offered by Output 1 but smaller than the minimum delay offered by Output 2. Thus, in the case where the downstream user of the delayed signals can access whichever tap they choose (e.g. via MEMS switches) the circuit can offer nearly continuous delay coverage between approximate $[270, 600]ps$ throughout its operating range, corresponding to phase delays between $[180, 400]degree$ at 1.6GHz.

The minimum tuneable steps of the delay time at each output port with different memristor values are shown in Table VI. As the uncertainties of the delay circuit are compounded across the cascade architecture, the worst minimum delay step is at Output 3 with memristor value 10kΩ, which is $8.7ps$, equals to 1.4% of the delay at that output port with that memristor value. The smallest minimum step is at Output 1 with memristor value 17kΩ, the value is $0.4ps$ and equals to 0.15% of the delay time at that output port and memristor resistance. It can be observed that with the same memristor value, the minimum delay step in Output 2 is a little higher than twice the minimum step in Output 1. This is because the signal connection wires and capacitors in between different delay stages also add small delay values to the signal.

The total harmonic distortion (THD) results of the GHz delay circuit are shown in Fig 6. With the same memristor

TABLE V
GAIN, PHASE AND DELAY OF THE GHz DELAY CIRCUIT

	Gain (dB)	Phase (deg) @1.6GHz	Delay (ps) @1.6GHz
Out 1	-1.7 ~ -0.1	-154 ~ -191	269 ~ 335
Out 2	-1.7 ~ 0.1	-212 ~ -268	373 ~ 470
Out 3	-1.9 ~ 1.1	-270 ~ -360	474 ~ 632

TABLE VI
MINIMUM DELAY STEP OF THE GHz DELAY CIRCUIT WITH DIFFERENT MEMRISTOR VALUE

Memristor (kΩ)	Out1 (ps)	Out2 (ps)	Out3 (ps)
10	2.7	5.7	8.7
11	2.3	4.7	7.4
12	1.8	3.9	6.2
13	1.4	2.9	4.8
14	1.1	2.3	3.8
15	0.8	1.8	2.9
16	0.6	1.3	2.2
17	0.4	0.9	1.5

TABLE VII
MONTE CARLO ANALYSIS RESULTS OF THE GHz DELAY CIRCUIT

	Mean	Max	Min	Std Dev
Max gain (dB)	1.1	2.31	-1.33	0.6
Min gain (dB)	-1.9	1.58	-6	1.22
Max delay (ps)	633	892	415	80
Min delay (ps)	255	301	199	17

value, Output 3 has the largest distortion while Output 1 has the lowest distortion. For all the output ports, output signals with larger delay values, which also have lower memristor values, have worse distortion curves. This is because when the input DC voltage is low, the transconductance of the transistor is also low, which makes the harmonic distortion worse. To guarantee $THD < 10\%$, the input signal amplitude should always be $< 30mV$.

Monte Carlo analysis results are shown in Table 6. The min/max gain and delay data are collected at a frequency of

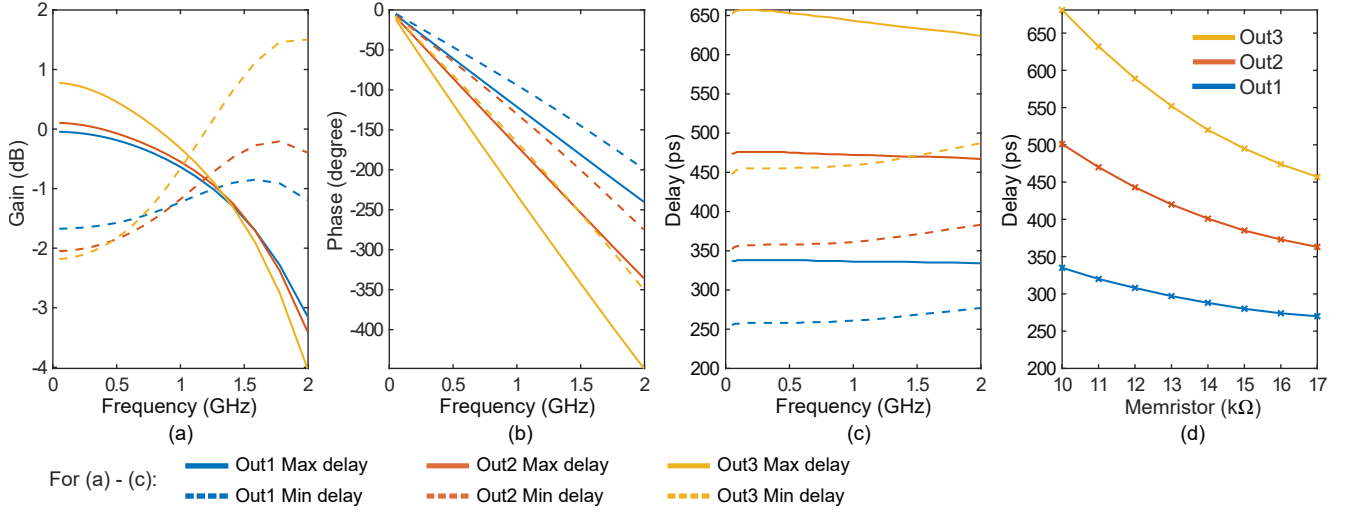


Fig. 5. (a) Gain, (b) phase and (c) delay time of the GHz delay circuit. Gain varies from -2 to 1dB in the whole GHz delay circuit. The delay offered by the GHz circuit at 1.6GHz is [269, 632]ps, except a space between 335ps and 373ps can not be covered by the delay circuit. (d) The delay time with different memristor values at 1.6GHz.

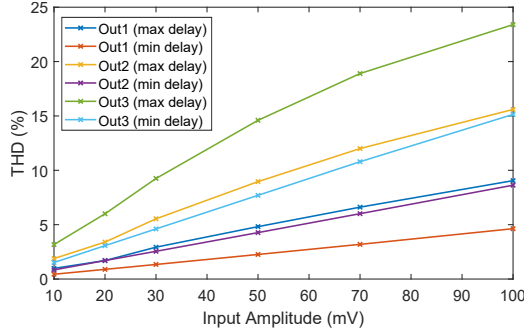


Fig. 6. Total harmonic distortion of the GHz delay circuit. Signal distortion increases with the cascade output port number. To make sure all the output ports have signal distortion smaller than 10%, the input signal amplitude should be smaller than 30mV.

TABLE VIII

CORNER, TEMPERATURE AND VOLTAGE SUPPLY VARIATION ANALYSIS OF GHz DELAY CIRCUIT. SEE TEXT FOR MODIFIED VERSIONS.

	Gain(dB)	Delay(ps)	Bandwidth(Hz)
Normal	-1.9 ~ 1.1	269 ~ 632	50M ~ 1.6G
ff	-6.3 ~ -1.1	230 ~ 461	None
ff (modified)	-4 ~ -1	239 ~ 471	50M ~ 2.1G
ss	-0.9 ~ 2.1	335 ~ 1126	50M ~ 550M
T: -20°C	-2 ~ 1	258 ~ 664	50M ~ 1.2G
T: 85°C	-3.6 ~ -0.5	299 ~ 677	None
T: 85°C (modified)	-3.2 ~ -0.5	299 ~ 656	50M ~ 1.25G
VDD 1.7V	-3 ~ 0	288 ~ 675	50M ~ 1.26G
VDD 1.9V	-2.5 ~ 0.5	272 ~ 627	50M ~ 1.41G

1.6GHz. As the variation of DC input voltage caused by the Monte Carlo analysis of memristor-based DC source can be reduced by adjusting the V_n voltage of DC source, in this simulation, the DC input voltages were chosen to be constant

values [605mV, 695mV, 711mV], which are the nominal voltage outputs of the DC source when memristor is 11kΩ, 16kΩ and 17kΩ. In these three values, input voltage 605mV corresponds to the maximum delay and the minimum gain at 1.6GHz in Output 3; Input voltage 695mV corresponds to the maximum gain at 1.6GHz in Output 3, and input voltage 711mV corresponds to the minimum delay in Output 1. The standard deviation (σ) shows the variation of the data. The ratio of [Std Dev/ Mean value] for the maximum delay is 12.6%, and for the minimum delay is 6.7%. Results show the minimum value of the maximum delay time is 415ps, and the maximum value of the minimum delay is 301ps. As the period at 1.6 GHz is 625ps, the delay circuit can always offer phase shift around 173° to 239° at 1.6GHz. It can be found the minimum gain and maximum delay values have larger variations, which is because they are measured with low input DC voltage. When input DC voltage is low, a small variation in DC voltage can generate a large change of gain and delay in the output signal.

The corner, temperature, and voltage supply variation analysis results are shown in Table VIII. As with the Monte Carlo simulation setting above, the data in Table VIII is collected in the condition when fixed DC voltage is applied on the input of delay circuit with value [605mV, 695mV, 711mV]. Results show that transistor corners strongly affect the performance of the circuit, while temperature and supply voltage variation have a smaller influence. Transistor corner ff increases the gain variation and the cut-off frequency, but reduces the gain value, delay value and delay variation range. Corner ss reduces the gain variation at low frequency and the cut-off frequency, but increases the gain value, offers a larger delay value and delay range. In this simulation, the gain variation of the ff corner and temperature 85 °C become larger than 3dB at all frequencies, hence at the chosen bias voltages the operating bandwidth is reduced to 0. To deal with the large gain variation caused by ff corner, the input voltage range needs to be reduced. The

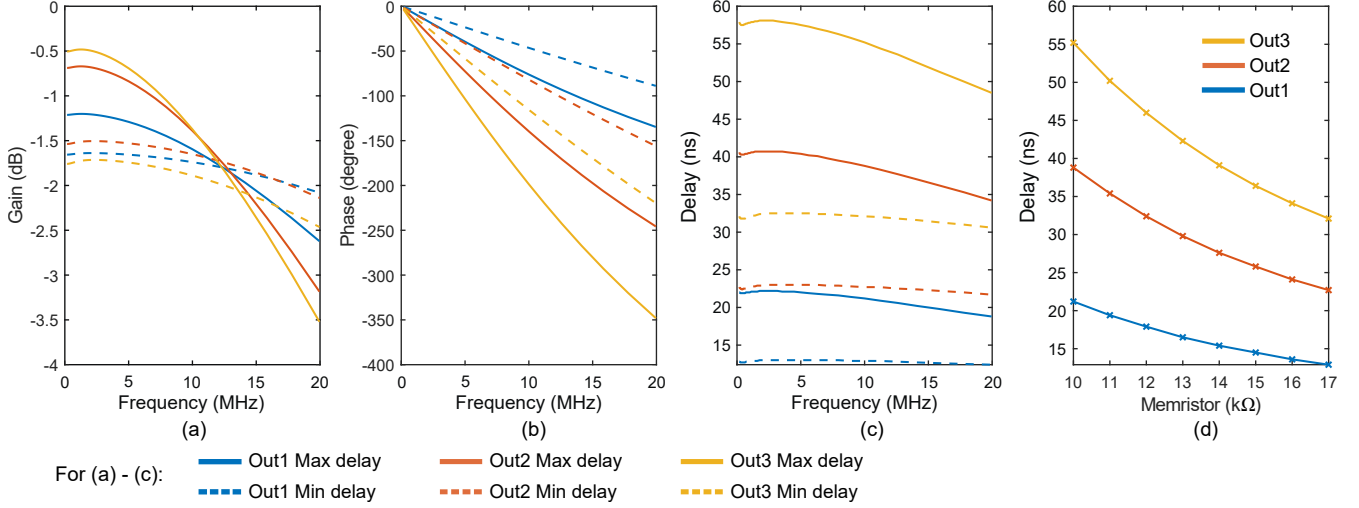


Fig. 7. (a) Gain, (b) phase and (c) delay time of the MHz delay circuit. This MHz delay circuit is assumed to work at 10MHz. The circuit has a gain variation of [-1.89, -0.5]dB from 200k to 10MHz, and offers a delay range of [13, 55]ns at 10MHz. (d) The delay time with different memristor values at 10MHz.

green regions show the results of ff corner simulated with input voltage [0.59, 0.65]V, and the circuit at temperature 85°C with input voltage [0.6, 0.69]V. Both of the changed input ranges are affordable for the memristor-based DC voltage source. Combined with the Monte Carlo analysis results above, it shows the process variation in transistor functions is one of the largest problems in the performance reduction of the GHz delay circuit.

The area of the GHz delay circuit is $164 \times 181 \mu m^2$, in which the 3 stages delay elements have an area of $82 \times 104 \mu m^2$, while the rest of the area is occupied by the GHz output buffers. The power consumption of the GHz delay part with memristor value [10kΩ, 17kΩ] are [7.56mW, 18mW], and the power consumption of one GHz output buffer is 68.4mW. To reduce power consumption, the output buffers in the delay circuits can be turned off when the output ports of these buffers are not used.

C. Result of MHz Delay Elements

The W/L of transistors $M1$ to $M4$ in the MHz delay elements are $12 \mu m / 2 \mu m$, while the W/L of $M5$ is $24 \mu m / 2 \mu m$, and the value of capacitor $C1$ is 33fF. The MHz delay circuit and the GHz delay circuit have the same $C1$ capacitance value, to eliminate the difference of performance caused by the capacitors. The gain, phase and delay data of the MHz delay element part are recorded in Fig 7 and Table IX. All data in Table IX is collected with a 10MHz input signal. As the gain variation of the MHz delay circuit is smaller than the GHz circuit, all three ports of the MHz circuit can use the full resistance variation range [10kΩ, 17kΩ] of the memristor to generate a larger delay range. The -3dB frequency of the MHz circuit is around 23MHz, well above the design operating frequency of 10MHz. Table IX shows that the whole 10MHz delay circuit offers -46° to -198° phase shift, which equals to 13ns to 55ns time delay at 10MHz, with gain variation from -1.89dB to -0.5dB. The tuneable phase shift range is 152° .

TABLE IX
GAIN, PHASE AND DELAY OF THE MHZ DELAY CIRCUIT

	Gain (dB)	Phase (degree)	Delay (ns)
Out 1	-1.74 ~ -1.2	-46 ~ -76	13 ~ 21
Out 2	-1.65 ~ -0.68	-81 ~ -140	23 ~ 38
Out 3	-1.89 ~ -0.5	-115 ~ -198	32 ~ 55

TABLE X
MINIMUM DELAY STEP OF THE MHZ DELAY CIRCUIT AT DIFFERENT MEMRISTOR VALUE

Memristor (kΩ)	Out1 (ns)	Out2 (ns)	Out3 (ns)
10	0.32	0.62	0.89
11	0.27	0.52	0.74
12	0.21	0.41	0.59
13	0.18	0.35	0.51
14	0.1	0.2	0.29
15	0.09	0.17	0.25
16	0.09	0.17	0.24
17	0.05	0.1	0.15

TABLE XI
MONTE CARLO ANALYSIS RESULTS OF THE MHZ DELAY CIRCUIT

	Mean	Max	Min	Std Dev
Max gain (dB)	-0.5	0.36	-1.56	0.36
Min gain (dB)	-1.96	-0.96	-3.16	0.4
Max delay (ns)	55	66	48	2.9
Min delay (ns)	13.7	15.5	12.6	0.5

The delay resolutions of the MHz delay circuit at different memristor values are recorded in Table X. The best delay resolution is at Output 1 with memristor 17kΩ, yielding 0.38% of the delay. The worst delay minimum step is at Output 3 with the memristor at 10kΩ, yielding 1.62% of the delay value.

The MHz THD results are shown in Fig 8. Similar to the trend of GHz THD curves, with higher stages of output port and lower memristor value, the THD values are also higher. To make sure the THD < 10% in all the conditions, the input signal amplitude should be smaller than 20mV.

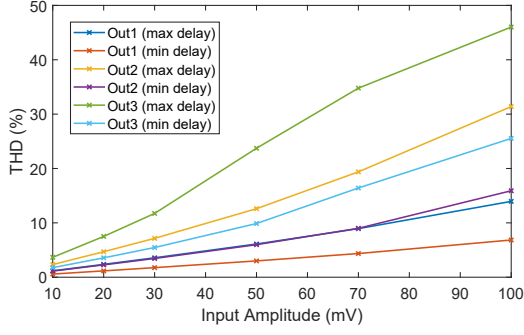


Fig. 8. Total harmonic distortion of the MHz delay circuit. To make sure the signal distortion is smaller than 10% in all the output ports, the input signal amplitude should be smaller than 20mV.

TABLE XII
CORNER, TEMPERATURE AND VOLTAGE SUPPLY VARIATION ANALYSIS OF
MHZ DELAY CIRCUIT

	Gain (dB)	Delay (ns)	Bandwidth (Hz)
Normal	-1.89 ~ -0.5	13 ~ 55	40k ~ 23M
ff	-3.6 ~ -2.3	12 ~ 48	40k ~ 28M
ss	-0.35 ~ 1	15 ~ 63	40k ~ 18M
T: -20°C	-2.37 ~ -0.05	13 ~ 55	40k ~ 23M
T: 80°C	-2.65 ~ -0.95	15 ~ 57	40k ~ 20M
VDD 1.7V	-2.45 ~ -0.2	14 ~ 57	40k ~ 23M
VDD 1.9V	-2.5 ~ -0.64	14 ~ 56	40k ~ 23M

The Monte Carlo simulation results of the 10 MHz delay circuit are recorded in Table XI. Results show that gain variation remains low (well within 3dB). The minimum delay of the delay circuit has a change smaller than 1.8ns, but the maximum delay value varies up to 11ns. In the worst case, the delay circuit may not be able to offer 50ns delay time, which equals to 180° phase shift at 10 MHz. The standard deviation results of the gain value in the MHz circuit are much better than the GHz circuit. One of the main reasons is the circuit works at a lower frequency and is therefore less influenced by parasitic capacitance. Another reason is the cut-off frequency of the MHz circuit is at around 20MHz, while the Monte Carlo analysis of the circuit was done at 10MHz. Finally, the gain variation of the MHz delay circuit at low frequency is smaller compared to the GHz circuit, which means the input DC voltage range in this research has not reached the extreme working condition of the MHz circuit.

The transistor corner, temperature variation and voltage supply variation analysis results are recorded in Table XII. The delay and bandwidth vary in a small range, the circuit being able to reliably restrict gain within [0, -3]dB, support delays between [15-48]ns and cover a bandwidth of [40k, 18MHz]. The gain variation in percentage is larger compared with the delay and bandwidth but still affordable. It is found the MHz circuit has better stability than the GHz circuit when dealing with transistor corner effect, variation of temperature and supply voltage.

The area of the MHz delay circuit is $104 \times 138 \mu m^2$. The power consumption of the MHz delay part with memristor value [10kΩ, 17kΩ] is [398μW, 954μW], while the power of each MHz output buffer is 4.6mW.

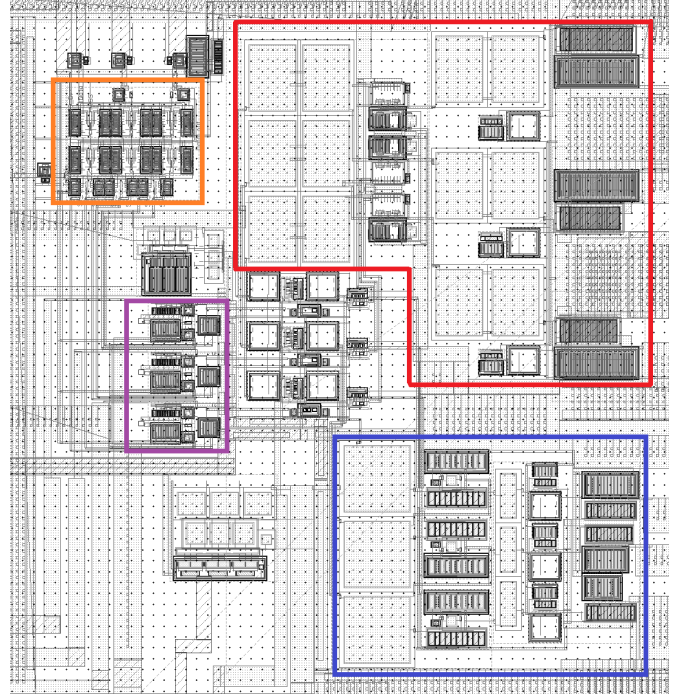


Fig. 9. Layout of the memristor-based tuneable delay core circuits. The red region is the GHz delay circuit, the blue region is the MHz delay circuit, the purple region is the memristor-based DC voltage sources, and the orange region is the memristor-programming controller.

D. Overview of the Delay Circuit

Fig 9 shows the layout of the memristor-based tuneable delay circuit core circuit excluding the pad ring. The area of the tuneable delay core circuit is $283 \times 290 \mu m^2$. The area framed in red is the GHz delay circuit including the output buffers, and the area framed in blue is the MHz delay circuit. The purple region is the memristor-based DC voltage sources which include the memristor devices, and the orange region is the memristor-programming controller. Other parts in the circuit include the switches between delay circuits and DC sources, and the oscillators to generate 1.6GHz and 10MHz input signals for the delay circuits. The main power consumption of the whole circuit is in the GHz output buffers. As expected, the GHz circuit uses much more power than the MHz circuit. The power consumption with a memristor value 17kΩ is larger than the power with a 10kΩ memristor because the memristor value controls the input gate voltage of the transistors in delay elements, thus controls the drain currents flowing through the delay circuits indirectly.

IV. DISCUSSION

Comparing the data of the GHz delay circuit with the MHz delay circuit, it is found that both the maximum and the minimum phase shift offered by the GHz delay circuit are larger than the MHz circuit. For the maximum phase shift, the reason is the data is simulated with 10MHz frequency signals while the cut-off frequency of the MHz delay circuit is around 23MHz. For the minimum phase shift, this result is mainly caused by the peripheral circuits of the GHz delay elements, including the output buffers, wide connecting wires,

TABLE XIII
COMPARISON BETWEEN THE WORKS IN THIS RESEARCH AND OTHER LITERATURE

	[29]	[33]	[34]	[35]	This Work (GHz)	This work (MHz)
Technology	0.14 μ m CMOS	65nm CMOS	0.13 μ m CMOS	65nm CMOS	0.18 μ m CMOS	0.18 μ m CMOS
Supply Voltage (V)	1.5	1.2	1.5	1.2	1.8	1.8
Gain (dB)	12 ~ 15	-4.5 ~ -0.8	5 ~ 11	-4.8 ~ 7.4	-2 ~ 1	-1.9 ~ -0.5
Gain Variation (dB)	± 1.4	± 0.5	± 3	0.14	± 1.5	± 1.2
Max. Delay (ps)	550	2000	225	1000	632	55000
Frequency (Hz)	1G ~ 2.5G	0.1G ~ 0.5G	1G ~ 15G	0.2G ~ 3G	0.05G ~ 1.6G	0.2M ~ 10M
Delay Variation	1.8%	0.5%	14%	1%	4.1%	5.4%
Power (mW)	90	9.6	78	30	76 ~ 86	5 ~ 5.6
Resolution (ps)	13	-	15	2	0.4 ~ 8.7	50 ~ 890
Size (mm^2)	0.07	0.12	1.5	0.185	0.052	0.05

electrostatic discharge devices (ESD) and the pad ring around the whole circuit. When the signal flows through the buffers and the pads, there are delays added to the signal. Besides, the parasitic capacitance of the peripheral circuits will also reduce the gain and increase the delay time of the delay circuit. For a delay circuit works in 10MHz and output delay time in the range of ns, the effect of peripheral circuits is not obvious. However, for GHz delay elements that offer ps delay, the delay time caused by the peripheral devices is very significant.

The THD values of the MHz circuit are fully larger than the data of the GHz circuit at the same signal amplitude and same output port. This is currently attributed to the smaller width/length ratio of transistors $M1$ to $M5$ (and therefore smaller transconductance g_m) required for MHz operation. Part of the effect can also be attributed to the MHz circuit using the full [10k Ω , 17k Ω] memristor range for DC voltage input, when the GHz circuit only uses memristor value 11k Ω for the maximum delay value, improving its THD figure. The smaller transconductance value in the transistor $M1$ to $M5$ increases the harmonic distortion of the MHz circuit.

The performance comparison results of the GHz delay circuit in this paper with other delay circuits are shown in Table XIII. Both the size data of the GHz and MHz work include the area of memristor-based DC source, memristor programming controller and the oscillators for input signal generation. The delay circuit in this research uses a small area, and reaches very fine delay resolution when the output delay time is low. When the output delay value is high, the resolution reduces but also remains relatively high compared with other designs. The resolution of the design in this research changes as the delay time changes with the memristor value non-linearly. The power of this design also varies in a range, because the input DC voltages of delay elements change and vary the currents in the circuits.

There are still aspects that can be optimized. First, the delay range of this delay circuit strongly relates to the voltage V_n in the memristor-based DC voltage source, as shown in Fig 1a. Even if circuit performance is affected by the environment, by changing V_n the output DC voltage of the tuneable DC source can be adjusted to a suitable range restoring function. However, it also means the accuracy of voltage V_n needs to be very high, otherwise the variation of V_n will change the performance of the circuit. On the other hand, engineers still necessary to caliber the V_n value by themselves, which makes the operation of this circuit more complex. To solve

these problems, an automatic negative feedback circuit that can adjust the output range of DC sources might be helpful. As memristors show varying static resistance as a function of bias voltage, it might be possible to use memristors to design such a feedback circuit. Second, the circuit is designed to be able to choose one of the three output buffers open and the other two close for lower power consumption, i.e. different delay ranges are made available at different, buffered output ports. A better method may be to use only one buffered output port, with a switch circuit to select which tap controls the buffer. The challenge in this method is designing high-frequency switches. They also need low gain distortion to allow high-speed signal pass when they turn on, and isolate the signal effectively to avoid signal mixing via cross-talk. Third, this delay circuit cascades three 1st-order all-pass filters. This method helps expand the delay range, but does not make the whole delay circuit become a higher order filter. To improve the circuit structure, the 3-stage delay circuits can include one 1st-order all-pass filter and two 2nd-order all-pass filter, to generate a 5th-order all-pass filter. These three directions can be considered to improve the design in further work.

V. CONCLUSION

In this paper, a reconfigurable delay circuit controlled by memristor-based DC voltage sources is reported. The memristor-based DC source offers DC voltage from 584mV to 711mV with high resolution. The delay circuit works in frequency range from 50MHz to 1.6GHz, and it offers an output delay range from 269ps to 632ps, with only 0.4ps minimum resolution. A delay circuit working at low MHz was also simulated to compare with the GHz circuit. Compared with other tunable true time delay designs, the tuneable GHz delay circuit in this research is designed based on 180nm CMOS technology, but shows a small size, and a very fine minimum delay step which is smaller than most of the other true time tuneable delay circuits. This work also includes the memristor programming circuit for changing the memristor resistance. This research shows the potential of memristors in reconfigurable analogue and RF devices: by using memristors in tuneable voltage or current sources, and designing circuits that can be controlled by voltage/current, memristors can introduce elegant and fine-grained reconfigurability even in circuits operating at very high frequencies.

VI. REFERENCE

- [1] Ali Hajimiri et al. "Integrated phased array systems in silicon". In: *Proceedings of the IEEE* 93.9 (2005), pp. 1637–1655.
- [2] Don Parker and David C Zimmermann. "Phased arrays-part 1: theory and architectures". In: *IEEE transactions on microwave theory and techniques* 50.3 (2002), pp. 678–687.
- [3] Zhang Rongzhi and Yang Kaizhong. *Spacecraft collision avoidance technology*. Academic Press, 2020.
- [4] Ruth Rotman, Moshe Tur, and Lior Yaron. "True time delay in phased arrays". In: *Proceedings of the IEEE* 104.3 (2016), pp. 504–518.
- [5] Matt Longbrake. "True time-delay beamsteering for radar". In: *2012 IEEE National Aerospace and Electronics Conference (NAECON)*. IEEE. 2012, pp. 246–249.
- [6] Istvan Frigyes and AJ Seeds. "Optically generated true-time delay in phased-array antennas". In: *IEEE Transactions on Microwave Theory and Techniques* 43.9 (1995), pp. 2378–2386.
- [7] Julien Perruisseau-Carrier et al. "Modeling of periodic distributed MEMS-application to the design of variable true-time delay lines". In: *IEEE Transactions on Microwave Theory and Techniques* 54.1 (2006), pp. 383–392.
- [8] Peigen Yu and Dixian Zhao. "Design Considerations for Wideband Hybrid Large-Scale Antenna Array and Implementation of a 5–23-GHz CMOS True-Time-Delay Circuit". In: *IEEE Transactions on Circuits and Systems II: Express Briefs* (2023).
- [9] Aravind Nagulu et al. "A full-duplex receiver with true-time-delay cancelers based on switched-capacitor-networks operating beyond the delay–bandwidth limit". In: *IEEE Journal of Solid-State Circuits* 56.5 (2021), pp. 1398–1411.
- [10] Mohammad Hossein Ghazizadeh and Ali Medi. "Novel trombone topology for wideband true-time-delay implementation". In: *IEEE Transactions on Microwave Theory and Techniques* 68.4 (2019), pp. 1542–1552.
- [11] Scott Barker and Gabriel M Rebeiz. "Distributed MEMS true-time delay phase shifters and wide-band switches". In: *IEEE Transactions on Microwave Theory and Techniques* 46.11 (1998), pp. 1881–1890.
- [12] Feng Hu and Koen Mouthaan. "A 1–20 GHz 400 ps true-time delay with small delay error in 0.13 μm CMOS for broadband phased array antennas". In: *2015 IEEE MTT-S International Microwave Symposium*. IEEE. 2015, pp. 1–3.
- [13] Sanggu Park and Sanggeun Jeon. "A 15–40 GHz CMOS true-time delay circuit for UWB multi-antenna systems". In: *IEEE microwave and wireless components letters* 23.3 (2013), pp. 149–151.
- [14] Imon Mondal and Nagendra Krishnapura. "A 2-GHz Bandwidth, 0.25–1.7 ns True-Time-Delay Element Using a Variable-Order All-Pass Filter Architecture in 0.13 μm CMOS". In: *IEEE Journal of Solid-State Circuits* 52.8 (2017), pp. 2180–2193.
- [15] Yang Chen and Wenyuan Li. "Compact and broadband variable true-time delay line with DLL-based delay-time control". In: *Circuits, Systems, and Signal Processing* 37 (2018), pp. 1007–1027.
- [16] Min Li et al. "An 800-ps origami true-time-delay-based CMOS receiver front end for 6.5–9-GHz phased arrays". In: *IEEE Solid-State Circuits Letters* 3 (2020), pp. 382–385.
- [17] Mohammad Hossein Ghazizadeh and Ali Medi. "A 125-ps 8–18-GHz CMOS integrated delay circuit". In: *IEEE Transactions on Microwave Theory and Techniques* 67.1 (2018), pp. 162–173.
- [18] Leon Chua. "Memristor-the missing circuit element". In: *IEEE Transactions on circuit theory* 18.5 (1971), pp. 507–519.
- [19] Dmitri B Strukov et al. "The missing memristor found". In: *nature* 453.7191 (2008), p. 80.
- [20] Dongqing Liu et al. "Nonvolatile bipolar resistive switching in amorphous Sr-doped LaMnO₃ thin films deposited by radio frequency magnetron sputtering". In: *Applied Physics Letters* 102.13 (2013).
- [21] Spyros Stathopoulos et al. "Multibit memory operation of metal-oxide bi-layer memristors". In: *Scientific reports* 7.1 (2017), p. 17532.
- [22] Omid Kavehei et al. "The fourth element: characteristics, modelling and electromagnetic theory of the memristor". In: *Proceedings of the Royal Society A: Mathematical, Physical and Engineering Sciences* 466.2120 (2010), pp. 2175–2202.
- [23] Andy Thomas. "Memristor-based neural networks". In: *Journal of Physics D: Applied Physics* 46.9 (2013), p. 093001.
- [24] Mohammed Affan Zidan et al. "Memristor-based memory: The sneak paths problem and solutions". In: *Microelectronics journal* 44.2 (2013), pp. 176–183.
- [25] Vasileios Manouras et al. "Frequency response of metal-oxide memristors". In: *IEEE Transactions on Electron Devices* 68.7 (2021), pp. 3636–3642.
- [26] Seyed Kasra Garakoui et al. "Time delay circuits: A quality criterion for delay variations versus frequency". In: *Proceedings of 2010 IEEE International Symposium on Circuits and Systems*. IEEE. 2010, pp. 4281–4284.
- [27] Ahmet Çağr Ulusoy, Bernd Schleicher, and Hermann Schumacher. "A tunable differential all-pass filter for UWB true time delay and phase shift applications". In: *IEEE Microwave and Wireless Components Letters* 21.9 (2011), pp. 462–464.
- [28] Mohamed B Elamien et al. "A wideband delay-tunable fully differential allpass filter in 65-nm CMOS technology". In: *2019 IEEE International Symposium on Circuits and Systems (ISCAS)*. IEEE. 2019, pp. 1–5.
- [29] Seyed Kasra Garakoui et al. "Compact cascadable gm-C all-pass true time delay cell with reduced delay variation over frequency". In: *IEEE journal of solid-state circuits* 50.3 (2015), pp. 693–703.

- [30] Behzad Razavi. “Prospects of CMOS technology for high-speed optical communication circuits”. In: *IEEE journal of solid-state circuits* 37.9 (2002), pp. 1135–1145.
- [31] Thomas H Lee. *The design of CMOS radio-frequency integrated circuits*. Cambridge university press, 2003.
- [32] Ioannis Messaris et al. “A data-driven verilog-a reram model”. In: *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems* 37.12 (2018), pp. 3151–3162.
- [33] Erez Zolkov et al. “Analysis and design of N-path true-time-delay circuit”. In: *IEEE Transactions on Microwave Theory and Techniques* 68.12 (2020), pp. 5381–5394.
- [34] Ta-Shun Chu, Jonathan Roderick, and Hossein Hashemi. “An Integrated Ultra-Wideband Timed Array Receiver in 0.13 μm CMOS Using a Path-Sharing True Time Delay Architecture”. In: *IEEE Journal of solid-state circuits* 42.12 (2007), pp. 2834–2850.
- [35] Erez Zolkov and Emanuel Cohen. “A 0.2–3-GHz N-path true time delay circuit achieving $< 1\%$ delay variation over frequency”. In: *IEEE Transactions on Microwave Theory and Techniques* 70.6 (2022), pp. 3224–3233.